TEXAS INSTRUMENTS

Amplifiers and Comparators

Data Book
New Releases

2000

Analog and Mixed Signal

Amplifiers and Comparators
Data Book

New Releases

Literature Number: SLOD002

TEXAS INSTRUMENTS

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INTRODUCTION

As the world leader in DSP and Analog, Texas Instruments (TI) designs, manufactures, and markets a broad portfolio of operational amplifiers and comparators in addition to many other integrated products. TI offers *thousands* of amplifiers to suit a broad range of application needs. This databook of new releases represents the first of three lines of amplifiers at TI:

- Amplifiers and Comparators
- Audio Power Amplifiers
- High Speed Amplifiers

How Amplifiers information is organized

The 1997 databook *Amplifiers, Comparators and Special Functions*, in two volumes (A & B), remains as a reference. This supplement is the year 2000 Databook of new releases, *Amplifiers and Comparators*, and includes all new releases of performance amplifiers since 1997. New releases of Audio Power Amplifiers can be found in a separate volume, entitled *Audio Power Amplifiers*, also published in 2000. And new releases of High Speed Amplifiers are found in another databook entitled *High Speed Amplifiers*, also released in 2000.

There is an alphanumeric index and selection guide within this volume. This databook includes selection guides sorted by several criteria: speed, precision, low power, micropower, low noise, rail-to-rail, and low voltage amplifiers. The selection guide includes all of the amplifiers that TI offers, including new releases and those listed in the 1997 Volumes A and B. Selection guides for High Speed and Audio Power Amplifiers are included here as separate sections.

To obtain any of the three databooks that represent TI's total current offering as follows in *Related TI Publications*, call your local TI Sales office, distributors, or the TI Product Information Center as listed in the last page of this book.

World Wide Web

Visit our world wide web site at **http://www.ti.com** for rapid access to the latest technology. Future amplifiers include complete families of low-voltage, ultra-low-power, rail-to-rail input/output, and improved BiMOS amplifiers. Most families are offered with and without shutdown. Our web site offers up-to-the-minute information about TI and its products; such as datasheets, a product parametric search (a user-sortable selection guide), application notes, amplifier evaluation modules, an on-line product sampling system, and much more.

Related TI Publications

Publication	Literature Number
Operational Amplifiers and Comparators Data Book New Releases 2000	SLOD002
Audio Power Amplifiers Databook 2000	SLOD004
High Speed Amplifiers Databook 2000	SLOD005
August 1999 Mixed Signal and Analog Designer's Guide, including CD ROM of 1999 Designer's Guide and Databook	SLYU001B (updated biannually)
CD ROM of Mixed Signal Designer's Guide and Databook	SLYC005C (updated biannually)
Amplifiers, Comparators, and Special Functions 1997, Volume A	SLYD011A
Amplifiers, Comparators, and Special Functions 1997, Volume B	SLYD012A
1999 Semiconductor Group Package Outlines Reference Guide	SSYU001E

For the latest product information check **www.ti.com/sc**

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If you do not have access to the web, call the TI product information center or your local TI Sales office as listed on the last page of this volume for assistance in obtaining a CD ROM or hardcopy of these volumes.

While these volumes offer information only on the amplifier and comparator devices available from TI, complete technical data for upcoming analog or any other TI Semiconductor product is available from your nearest TI sales office (listed on the last page of this book), your local authorized distributor, or by writing directly to:

Texas Instruments Incorporated
Literature Response Center
P.O. Box 809066
Dallas, Texas 75380–9066
United States

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General Information

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The devices in **BOLD** type are in this data book.

† This device is in the Product Preview stage of development.

NOTES: 1. The device can be found in the High-Speed Amplifiers Data Book (Literature Number SLOD005).
2. The device can be found in the Audio Power Amplifiers Data Book (Literature Number SLOD004).

The devices in **BOLD** type are in this data book.
† This device is in the Product Preview stage of development.
NOTES: 1. The device can be found in the High-Speed Amplifiers Data Book (Literature Number SLOD005).
2. The device can be found in the Audio Power Amplifiers Data Book (Literature Number SLOD004).

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NOTES: 1: The device can be found in the High-Speed Amplifiers Data Book (Literature Number SLOD005).
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ALPHANUMERIC INDEX

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The devices in **BOLD** type are in this data book.
† This device is in the Product Preview stage of development.
NOTES: 1: The device can be found in the High-Speed Amplifiers Data Book (Literature Number SLOD005).
2. The device can be found in the Audio Power Amplifiers Data Book (Literature Number SLOD004).

INTRODUCTION TO THE SELECTION GUIDES

The following selection guides are designed to help you quickly identify which operational amplifiers best suit your needs. This section includes specification tables for each operational amplifier, sorted by primary performance category. This permits a quick comparison of key specifications. Also included in this section is a complete alphanumerically sorted list of all Texas Instruments advanced linear amplifiers with key specifications.

The following selection guides are separated into seven primary-selection categories:

- DC precision
- Noise
- Low power
- Micro power
- Low voltage
- Rail to rail
- Wide Bandwidth (Higher Speed)

These categories are then subdivided into secondary and tertiary groups combining performance indices. An understanding of what is meant by each term is helpful when choosing the right amplifier for your application.

DEFINITION OF TERMS

DC Precision

Precision refers to an amplifier's inherent dc errors, the input offset voltage (V_{IO}), its temperature coefficient (α_{VIO}), and long-term drift (ΔV_{IO}). In direct-coupled applications, these errors are amplified by the amplifier and carried through the system. The magnitude of the input offset voltage limits the minimum signal level that can be accurately measured. This document defines precision operational amplifiers as those having $V_{IO} \leq 1$ mV. In the precision-operational-amplifiers specification table, these operational amplifiers are sorted in ascending order of V_{IO}max at 25°C.

Noise

Noise in operational amplifiers typically has two components: voltage noise and current noise. Current noise is primarily a function of input bias currents (I_{IB}) and is negligible in JFET-input (BiFET) and CMOS amplifiers. Voltage noise (V_n) is noise generated by the amplifier due to the thermal noise of the channel resistance in JFET and CMOS amplifiers or the emitter resistance in bipolar amplifiers. Bipolar technology offers the lowest voltage noise and offers the greatest advantage when interfacing to low-impedance sources. As source impedance increases to about 10 kΩ, system noise is dominated by the thermal noise of the source and feedback resistances and selection of an amplifier is usually driven by other characteristics. At higher source impedances, the noise contribution due to the high-input currents of bipolar amplifiers becomes prohibitive and either a CMOS or BiFET amplifier should be chosen. Amplifiers in the low-noise operational amplifier sections have $V_n \leq$ 15 nV/$\sqrt{Hz}$. Current noise, though not specified, can be approximated by:

$$I_n \approx \sqrt{(2 \times q \times I_{IB})}, \text{ where } q = 1.6 \times 10^{-19}$$

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Low Power

Low power in this document refers to amplifiers whose quiescent currents are less than 1 mA per channel. This category is further broken down to delineate micropower amplifiers, or those with I_{CC} or $I_{DD} \leq 50$ µA. The supply current is specified under no-load conditions; the outputs neither sink nor source current. To minimize power consumption, unused amplifiers should be connected as unity-gain followers with their inputs grounded.

Low Voltage

Low-voltage amplifiers operate with V_{CC} or $V_{DD} \leq 3$ V. Some CMOS amplifiers operate with $V_{DD} = 1.4$ V. When using any supply voltage, you must ensure that input signals are within the common-mode input voltage range (V_{ICR}) of the device. To address the emerging 3-V device market, Texas Instruments has introduced a full line of 3-V operational amplifiers, the TLV series of devices.

Rail to Rail

Rail-to-rail operational amplifiers feature outputs that swing close to both the positive and negative supply rails. To achieve expected results, maintain loading conditions within the specified drive capability of the amplifier; output swing decreases as load increases.

Wide Bandwidth (Higher Speed)

Speed refers to an operational amplifier's slew rate (SR) and its bandwidth. Slew rate describes the ability of the amplifier's output to follow a large rapidly changing signal at its input, expressed in V/µs. Slew rate is a function of and inversely proportional to supply current (I_{CC} or I_{DD}); increased power consumption must often be traded for faster output response. BiFET amplifiers have traditionally offered the best speed performance, although new complementary bipolar technologies are gaining ground. The high-speed operational amplifiers in this selection guide have a bandwidth ≥ 2 MHz; the amplifiers' slew rate is included in the specification tables for reference. For amplifiers specifically developed for applications requiring high-speed signal conditioning, please refer to the *High Speed Amplifiers Data Book* (Literature number SLOD005)
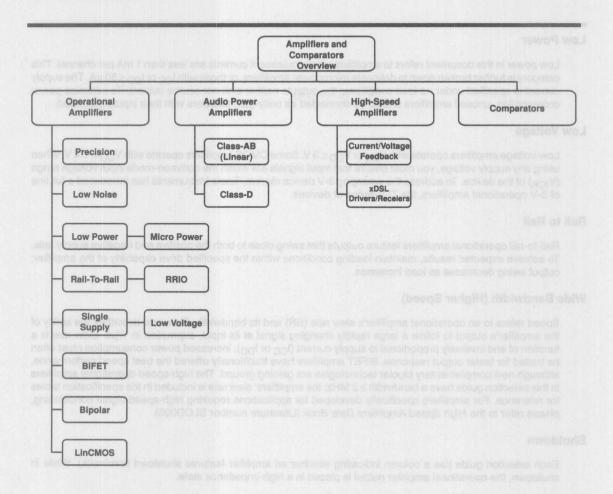
Shutdown

Each selection guide has a column indicating whether an amplifier features shutdown terminal(s). While in shutdown, the operational amplifier output is placed in a high-impedance state.

Single Supply

Single-supply operational amplifiers are those that are designed to operate well with only one power-supply rail, typically 5 V. They are generally characterized as having a common-mode input voltage range (V_{ICR}) that includes ground and outputs that can swing to or very near ground ($V_{OL} \approx 0$ V). Most single-supply operational amplifiers are manufactured using CMOS technology, although some bipolar single-supply amplifiers are available. Single-supply operational amplifiers can be used in systems with split supplies (e.g., ±5 V), but care must be taken not to exceed the maximum supply voltage across the device. For example, V_{DD}max for CMOS operational amplifiers is 16 V. No more than ±8 V should be applied to these devices in a split-supply system. Also, some single-supply operational amplifier output stages are not designed to both source and sink current; when used with split supplies, they may exhibit some crossover distortion as the signal passes through midsupply.

OPERATIONAL AMPLIFIER SELECTION GUIDE

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                        ┌─────────────────┐
                        │  Amplifiers and │
                        │   Comparators   │
                        │    Overview     │
                        └─────────────────┘
        ┌──────────────┬──────────┴──────────┬──────────────┐
┌───────────────┐ ┌──────────────┐ ┌──────────────┐ ┌──────────────┐
│  Operational  │ │ Audio Power  │ │  High-Speed  │ │ Comparators  │
│  Amplifiers   │ │  Amplifiers  │ │  Amplifiers  │ │              │
└───────────────┘ └──────────────┘ └──────────────┘ └──────────────┘
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- Operational Amplifiers
  - Precision
  - Low Noise
  - Low Power — Micro Power
  - Rail-To-Rail — RRIO
  - Single Supply — Low Voltage
  - BiFET
  - Bipolar
  - LinCMOS

- Audio Power Amplifiers
  - Class-AB (Linear)
  - Class-D

- High-Speed Amplifiers
  - Current/Voltage Feedback
  - xDSL Drivers/Recelers

- Comparators

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
LF347	36	7	2	2.75	13	10	50	100	18	3	13	4			±15	Vol. A
LF347B	36	7	2	2.75	7	5	50	100	18	3	13	4			±15	Vol. A
LF353	36	7	1.8	3.25	13	10	50	100	18	3	13	2			±15	Vol. A
LF411	36	7	2	3.4		2	50	100	18	3	13	1			±15	Vol. A
LF412	36	7	2.25	3.4		3	50	100	18	3	13	2			±15	Vol. A
LM2902	26	3	0.175	0.3	10	7	−20000	80	23	0.4	0.25	4			5	Vol. A
LM2904	26	3	0.35	0.6	10	7	−20000	80	23	0.4	0.15	2			5	Vol. A
LM318	40	10	5	10	15	10	150000	100	23	15	70	1			±15	Vol. A
LM324	32	3	0.175	0.3	9	7	−20000	80	23	0.4	0.25	4			5	Vol. A
LM324A	32	3	0.175	0.3	5	3	−15000	80	23	0.4	0.25	4			5	Vol. A
LM348	36	8	0.6	1.125	7.5	6	30000	90	23	1	0.5	4			±15	Vol. A
LM358	32	3	0.5	1	9	7	−20000	80	23	0.4		2			5	Vol. A
LM358A	32	3	0.5	1	5	3	−15000	80	23	0.4		2			5	Vol. A
LT1013	44	4	0.35	0.55	0.4	0.3	−15000	114	22		0.4	2			±15	Vol. A
LT1013A	44	4	0.35	0.5	0.24	0.15	−12000	117	22		0.4	2			±15	Vol. A
LT1013D	44	4	0.35	0.55	1	0.8	−15000	114	22		0.4	2			±15	Vol. A
MC1458	30	10	1.7	2.8	7.5	6	80000	90	45	1	0.5	2			±15	Vol. A
MC3403	30	5	0.7	1.75	12	10	−200000	90		1	0.6	4			±15	Vol. A
NE5532	30	10	4	8	5	4	200000	100	5	10	9	2			±15	Vol. A
NE5534	30	10	4	8	5	4	500000	100	4	10	13	1			±15	Vol. A
NE5534A	30	10	4	8	5	4	500000	100	3.5	10	13	1			±15	Vol. A
OP07C	36	6	2.7	5	0.25	0.15	±1800	120	9.8	0.6	0.3	1			±15	Vol. A
OP07D	36	6	2.7	5	0.25	0.15	±2000	110	9.8	0.6	0.3	1			±15	Vol. A
RC4136	30	10	1.25	2.825	7.5	6	140000	90	8	3	1.7	4			±15	Vol. A
RC4558	30	10	1.25	2.8	7.5	6	150000	90	8	3	1.7	2			±15	Vol. A
TL022	30	10	0.065	0.125	7.5	5	100000	72	50	0.5	0.5	2			±15	Vol. A
TL031	30	10	0.217	0.28	2.5	1.5	2	94	41	1.1	5.1	1			±15	Vol. A
TL031A	30	10	0.217	0.28	1.8	0.8	2	94	41	1.1	5.1	1			±15	Vol. A
TL032	30	10	0.211	0.28	2.5	1.5	2	94	41	1.1	5.1	2			±15	Vol. A
TL032A	30	10	0.211	0.28	1.8	0.8	2	94	41	1.1	5.1	2			±15	Vol. A
TL034	30	10	0.2175	0.28	6.2	4	2	94	43	1.1	5.1	4			±15	Vol. A
TL034A	30	10	0.2175	0.28	3.7	1.5	2	94	43	1.1	5.1	4			±15	Vol. A

Devices in **bold** are is this data book
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OPERATIONAL AMPLIFIERS (continued)

TEXAS INSTRUMENTS

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TL051	30	10	2.7	3.2	2.5	1.5	30	93	18	3.1	20	1			±15	Vol. A
TL051A	30	10	2.7	3.2	1.8	0.8	30	93	18	3.1	20	1			±15	Vol. A
TL052	30	10	2.4	2.8	2.5	1.5	30	93	19	3	20.7	2			±15	Vol. A
TL052A	30	10	2.4	2.8	1.8	0.8	30	93	19	3	20.7	2			±15	Vol. A
TL054	30	10	2.1	2.8	6.2	4	30	92	21	2.7	17.8	4			±15	Vol. A
TL054A	30	10	2.1	2.8	3.7	1.5	30	92	21	2.7	17.8	4			±15	Vol. A
TL061	36	7	0.2	0.25	20	15	30	86	42	1	3.5	1			±15	Vol. A
TL061A	36	7	0.2	0.25	7.5	6	30	86	42	1	3.5	1			±15	Vol. A
TL061B	36	7	0.2	0.25	5	3	30	86	42	1	3.5	1			±15	Vol. A
TL062	36	7	0.2	0.25	20	15	30	86	42	1	3.5	2			±15	Vol. A
TL062A	36	7	0.2	0.25	7.5	6	30	86	42	1	3.5	2			±15	Vol. A
TL062B	36	7	0.2	0.25	5	3	30	86	42	1	3.5	2			±15	Vol. A
TL064	36	7	0.2	0.25	20	15	30	86	42	1	3.5	4			±15	Vol. A
TL064A	36	7	0.2	0.25	7.5	6	30	86	42	1	3.5	4			±15	Vol. A
TL064B	36	7	0.2	0.25	5	3	30	86	42	1	3.5	4			±15	Vol. A
TL070	36	7	1.4	2.5	13	10	65	100	18	3	13	1			±15	Vol. A
TL071	36	7	1.4	2.5	13	10	65	100	18	3	13	1			±15	Vol. A
TL071A	36	7	1.4	2.5	7.5	6	65	100	18	3	13	1			±15	Vol. A
TL071B	36	7	1.4	2.5	5	3	65	100	18	3	13	1			±15	Vol. A
TL072	36	7	1.4	2.5	13	10	65	100	18	3	13	2			±15	Vol. A
TL072A	36	7	1.4	2.5	7.5	6	65	100	18	3	13	2			±15	Vol. A
TL072B	36	7	1.4	2.5	5	3	65	100	18	3	13	2			±15	Vol. A
TL074	36	7	1.4	2.5	13	10	65	100	18	3	13	4			±15	Vol. A
TL074A	36	7	1.4	2.5	7.5	6	65	100	18	3	13	4			±15	Vol. A
TL074B	36	7	1.4	2.5	5	3	65	100	18	3	13	4			±15	Vol. A
TL081	36	7	1.4	2.8	20	15	30	86	18	3	13	1			±15	Vol. A
TL081A	36	7	1.4	2.8	7.5	6	30	86	18	3	13	1			±15	Vol. A
TL081B	36	7	1.4	2.8	5	3	30	86	18	3	13	1			±15	Vol. A
TL082	36	7	1.4	2.8	20	15	30	86	18	3	13	2			±15	Vol. A
TL082A	36	7	1.4	2.8	7.5	6	30	86	18	3	13	2			±15	Vol. A
TL082B	36	7	1.4	2.8	5	3	30	86	18	3	13	2			±15	Vol. A
TL084	36	7	1.4	2.8	20	15	30	86	18	3	13	4			±15	Vol. A

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Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TL084A	36	7	1.4	2.8	7.5	6	30	86	18	3	13	4			±15	Vol. A
TL084B	36	7	1.4	2.8	5	3	30	86	18	3	13	4			±15	Vol. A
TL343	36	3	0.7	2.8	12	10	−200	90		1	1	1			±15	2–7
TL3472	36	4	3.5	4.5	12	10	100000	97	49	4	13	2			±15	2–13
TLC070	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1	Y		5	2–17
TLC070A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1	Y		5	2–17
TLC071	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC071A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC072	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC072A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC073	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	2	Y		5	2–17
TLC073A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	2	Y		5	2–17
TLC074	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4			5	2–17
TLC074A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4			5	2–17
TLC075	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4	Y		5	2–17
TLC075A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4	Y		5	2–17
TLC080	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1	Y		5	2–43
TLC080A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1	Y		5	2–43
TLC081	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1			5	2–43
TLC081A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1			5	2–43
TLC082	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2			5	2–43
TLC082A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2			5	2–43
TLC083	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2	Y		5	2–43
TLC083A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2	Y		5	2–43
TLC084	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4			5	2–43
TLC084A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4			5	2–43
TLC085	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4	Y		5	2–43
TLC085A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4	Y		5	2–43
TLC1078	16	1.4	0.01	0.017	0.8	0.45	0.6	95	68	0.085	0.032	2			5	Vol. A
TLC1079	16	1.4	0.01	0.017	1.2	0.85	0.6	95	68	0.085	0.032	4			5	Vol. A
TLC2201	16	4.6	1	1.5	0.6	0.5	1	110	8	1.8	2.5	1		RRO	5	Vol. A
TLC2201A	16	4.6	1	1.5	0.3	0.2	1	110	15	1.8	2.5	1		RRO	5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIER GENERAL SELECTION GUIDE

OPERATIONAL AMPLIFIERS (continued)

TEXAS INSTRUMENTS

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLC2201B	16	4.6	1	1.5	0.3	0.2	1	110	12	1.8	2.5	1		RRO	5	Vol. A
TLC2202	16	4.6	0.85	1.3	1.15	1	1	100	8	1.9	2.5	2		RRO	5	Vol. A
TLC2202A	16	4.6	0.85	1.3	0.65	0.5	1	100	15	1.9	2.5	2		RRO	5	Vol. A
TLC2202B	16	4.6	0.85	1.3	0.65	0.5	1	100	12	1.9	2.5	2		RRO	5	Vol. A
TLC2252	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2252A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2254	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLC2254A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLC2262	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2262A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2264	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2264A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2272	16	4.4	1.1	1.5	3	2.5	1	75	9	2.18	3.6	2		RRO	5	Vol. A
TLC2272A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	2		RRO	5	Vol. A
TLC2274	16	4.4	1.1	1.5	3	2.5	1	75	9	2.18	3.6	4		RRO	5	Vol. A
TLC2274A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	4		RRO	5	Vol. A
TLC251	16	1.4	0.675	1.6	12	10	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC251A	16	1.4	0.675	1.6	6.5	5	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC251B	16	1.4	0.675	1.6	3	2	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC252	16	1.4	0.7	1.6	12	10	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC252A	16	1.4	0.7	1.6	6.5	5	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC252B	16	1.4	0.7	1.6	3	2	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC254	16	1.4	0.775	1.8	12	10	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC254A	16	1.4	0.775	1.8	6.5	5	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC254B	16	1.4	0.775	1.8	3	2	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC25L2	16	1.4	0.01	0.017	12	10	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2A	16	1.4	0.01	0.017	6.5	5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2B	16	1.4	0.01	0.017	3	2	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L4	16	1.4	0.01	0.017	12	10	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4A	16	1.4	0.01	0.017	6.5	5	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4B	16	1.4	0.01	0.017	3	2	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25M2	16	1.4	0.105	0.28	12	10	0.6	91	32	0.525	0.43	2			5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLC25M2A	16	1.4	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC25M4	16	1.4	0.105	0.28	12	10	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC25M4A	16	1.4	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC25M4B	16	1.4	0.105	0.28	3	2	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC2652	16	3.8	1.5	2.4	0.004	0.003	4	140	23	1.9	3.1	1			±5	Vol. A
TLC2652A	16	3.8	1.5	2.4	0.002	0.001	4	140	35	1.9	3.1	1			±5	Vol. A
TLC2654	16	4.6	1.5	2.4	0.034	0.02	50	125	13	1.9	3.7	1			±5	Vol. A
TLC2654A	16	4.6	1.5	2.4	0.024	0.01	50	125	20	1.9	3.7	1			±5	Vol. A
TLC271	16	3	0.675	1.6	12	10	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC271A	16	3	0.675	1.6	6.5	5	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC271B	16	3	0.675	1.6	3	2	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC272	16	3	0.7	1.6	12	10	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC272A	16	3	0.7	1.6	6.5	5	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC272B	16	3	0.7	1.6	3	2	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC274	16	3	0.675	1.6	12	10	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC274A	16	3	0.675	1.6	6.5	5	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC274B	16	3	0.675	1.6	3	2	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC277	16	3	0.7	1.6	1.5	0.5	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC279	16	3	0.675	1.6	1.5	0.9	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC27L1	16	3	0.01	0.017	13	10	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC27L1A	16	3	0.01	0.017	7	5	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC27L1B	16	3	0.01	0.017	3.5	2	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC27L2	16	3	0.01	0.017	13	10	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L2A	16	3	0.01	0.017	7	5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L2B	16	3	0.01	0.017	3.5	2	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L4	16	3	0.01	0.017	12	10	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L4A	16	3	0.01	0.017	6.5	5	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L4B	16	3	0.01	0.017	3	2	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L7	16	3	0.01	0.017	2	0.5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L9	16	3	0.01	0.017	1.5	0.9	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27M2	16	3	0.105	0.28	13	10	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC27M2A	16	3	0.105	0.28	7	5	0.6	91	32	0.525	0.43	2			5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLC27M2B	16	3	0.105	0.28	3.5	2	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC27M4	16	3	0.105	0.28	12	10	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC27M4A	16	3	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC27M4B	16	3	0.105	0.28	3	2	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC27M7	16	3	0.105	0.28	2	0.5	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC27M9	16	3	0.105	0.28	1.5	0.9	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC4501	6	4	1	1.5	0.08	0.08	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4501A	6	4	1	1.5	0.04	0.04	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4502	6	4	1.25	3.5	0.1	0.1	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLC4502A	6	4	1.25	3.5	0.05	0.05	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLE2021	40	4	0.2	0.3	0.85	0.6	25000	110	15	2	0.65	1			5	Vol. B
TLE2021A	40	4	0.2	0.3	0.6	0.3	25000	110	30	2	0.65	1			5	Vol. B
TLE2021B	40	4	0.2	0.3	0.3	0.2	25000	110	30	2	0.65	1			5	Vol. B
TLE2022	40	4	0.225	0.3	0.8	0.6	35000	100	15	2.8	0.65	2			5	Vol. B
TLE2022A	40	4	0.225	0.3	0.55	0.4	33000	102	15	2.8	0.65	2			5	Vol. B
TLE2022B	40	4	0.225	0.3	0.4	0.3	33000	105	15	2.8	0.65	2			5	Vol. B
TLE2024	40	4	0.26	0.35	1.3	1.1	46000	90	15	2.8	0.7	4			5	Vol. B
TLE2024A	40	4	0.26	0.35	1.05	0.85	40000	92	15	2.8	0.7	4			5	Vol. B
TLE2024B	40	4	0.26	0.35	0.8	0.6	35000	95	15	2.8	0.7	4			5	Vol. B
TLE2027	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	13	2.8	1			±15	Vol. B
TLE2027AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	13	2.8	1			±15	Vol. B
TLE2037	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	50	7.5	1			±15	Vol. B
TLE2037AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	50	7.5	1			±15	Vol. B
TLE2061	36	7	0.29	0.35	4	3	4	90	40	2	3.4	1			±15	Vol. B
TLE2061A	36	7	0.29	0.35	3.5	2.6	4	90	40	2	3.4	1			±15	Vol. B
TLE2061B	36	7	0.29	0.35	2.4	1.9	4	90	40	2	3.4	1			±15	Vol. B
TLE2062	36	7	0.31	0.345	4.9	4	4	90	40	2	3.4	2			±15	Vol. B
TLE2062A	36	7	0.31	0.345	2.9	2	4	90	40	2	3.4	2			±15	Vol. B
TLE2062B	36	7	0.31	0.345	1.9	1	4	90	40	2	3.4	2			±15	Vol. B
TLE2064	36	7	0.31	0.35	6.9	6	4	90	40	2	3.4	4			±15	Vol. B
TLE2064A	36	7	0.31	0.35	4.9	4	4	90	40	2	3.4	4			±15	Vol. B
TLE2064B	36	7	0.31	0.35	2.9	2	4	90	40	2	3.4	4			±15	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLE2071	38	4.5	1.7	2.2	6	4	20	98	14	10	45	1			±15	Vol. B
TLE2071A	38	4.5	1.7	2.2	4	2	20	98	14	10	45	1			±15	Vol. B
TLE2072	38	4.5	1.55	1.8	7.8	6	20	98	14	10	45	2			±15	Vol. B
TLE2072A	38	4.5	1.55	1.8	5.3	3.5	20	98	14	10	45	2			±15	Vol. B
TLE2074	38	4.5	1.425	1.875	7.1	5	25	98	14	10	45	4			±15	Vol. B
TLE2074A	38	4.5	1.425	1.875	5.1	3	25	98	14	10	45	4			±15	Vol. B
TLE2081	38	4.5	1.7	2.2	8	6	20	98	14	10	45	1			±15	Vol. B
TLE2081A	38	4.5	1.7	2.2	5	3	20	98	14	10	45	1			±15	Vol. B
TLE2082	38	4.5	1.55	1.8	8.1	7	20	98	14	10	45	2			±15	Vol. B
TLE2082A	38	4.5	1.55	1.8	5.1	4	20	98	14	10	45	2			±15	Vol. B
TLE2084	38	4.5	1.625	1.875	9.1	7	25	98	14	10	45	4			±15	Vol. B
TLE2084A	38	4.5	1.625	1.875	6.1	4	25	98	14	10	45	4			±15	Vol. B
TLE2141	44	4	3.5	4.5	1.3	0.9	−7000	108	10.5	5.9	45	1			±15	Vol. B
TLE2141A	44	4	3.5	4.5	0.8	0.5	−7000	108	10.5	5.9	45	1			±15	Vol. B
TLE2142	44	4	3.45	4.5	1.6	1.2	−7000	108	10.5	5.9	45	2			±15	Vol. B
TLE2142A	44	4	3.45	4.5	1.2	0.75	−7000	108	10.5	5.9	45	2			±15	Vol. B
TLE2144	44	4	3.45	4.5	3.2	2.4	−7000	108	10.5	5.9	45	4			±15	Vol. B
TLE2144A	44	4	3.45	4.5	2.4	1.5	−7000	108	10.5	5.9	45	4			±15	Vol. B
TLE2161	36	7	0.29	0.35	3.9	3	4	90	40	6.4	10	1			±15	Vol. B
TLE2161A	36	7	0.29	0.35	2.5	1.5	4	90	40	6.4	10	1			±15	Vol. B
TLE2161B	36	7	0.29	0.35	1	0.5	4	90	40	6.4	10	1			±15	Vol. B
TLE2227	38	8	3.65	5.3	0.5	0.35	15000	115	2.5	13	2.5	2			±15	Vol. B
TLE2301	40	9	2.2	3.5	15	10	260000	97	44	8	14	1			±15	Vol. B
TLV2211	10	2.7	0.013	0.025	3	0.45	1	83	22	0.065	0.025	1		RRO	5	Vol. B
TLV2221	10	2.7	0.11	0.15	3	0.45	1	85	19	0.51	0.18	1		RRO	5	Vol. B
TLV2231	10	2.7	0.85	1.2	3	0.45	1	70	15	2	1.6	1		RRO	5	Vol. B
TLV2252	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2252A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2254	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2254A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2262	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2262A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	2		RRO	5	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2264	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2264A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2322	8	2	0.01	0.017	11	9	0.6	94	68	0.027	0.02	2			5	Vol. B
TLV2324	8	2	0.01	0.017	12	10	0.6	94	68	0.027	0.02	4			5	Vol. B
TLV2332	8	2	0.1	0.28	11	9	0.6	91	32	0.3	0.38	2			5	Vol. B
TLV2334	8	2	0.1	0.28	12	10	0.6	91	32	0.3	0.38	4			5	Vol. B
TLV2341	8	2	0.675	1.6	10	8	0.6	80	25	1.7	3.6	1			5	Vol. B
TLV2342	8	2	0.325	1.5	11	9	0.6	80	25	0.79	2.1	2			5	Vol. B
TLV2344	8	2	0.325	1.5	12	10	0.6	78	25	0.79	2.1	4			5	Vol. B
TLV2361	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	1			±2.5	Vol. B
TLV2362	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	2			±2.5	Vol. B
TLV2422	10	2.7	0.05	0.075	2.5	2	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2422A	10	2.7	0.05	0.075	1.5	0.95	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2432	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	2		RRO	5	Vol. B
TLV2432A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	2		RRO	5	Vol. B
TLV2434	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	4		RRO	5	Vol. B
TLV2434A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	4		RRO	5	Vol. B
TLV2442	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2442A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2444	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLV2444A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLV2450	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2450A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2451	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2451A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2452	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2452A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2453	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2453A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2454	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2454A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2455	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

TEXAS
INSTRUMENTS

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2455A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2460	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2460A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2461	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2461A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2462	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2462A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2463	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2463A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2464	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2464A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2465	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2465A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2470	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2470A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1		RRIO	3	2–153
TLV2472	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2472A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2473	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2473A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2474	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2474A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2475	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2475A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2711	10	2.7	0.013	0.025	0.47	3	1	83	22	0.065	0.025	1		RRO	3	2–177
TLV2721	10	2.7	0.11	0.15	0.6	3	1	82	20	0.51	0.18	1		RRO	3	2–203
TLV2731	10	2.7	0.75	1.2	0.75	3	1	70	16	2	1.25	1		RRO	3	2–229
TLV2770	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2770A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2771	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1		RRO	2.7	2–255
TLV2771A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1		RRO	2.7	2–255

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

TEXAS INSTRUMENTS

OPERATIONAL AMPLIFIER GENERAL SELECTION GUIDE

OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2772	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2772A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2773	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2	Y	RRO	2.7	2–255
TLV2773A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2	Y	RRO	2.7	2–255
TLV2774	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4		RRO	2.7	2–255
TLV2774A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4		RRO	2.7	2–255
TLV2775	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4	Y	RRO	2.7	2–255
TLV2775A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4	Y	RRO	2.7	2–255
UA741	36	7	1.7	2.8	7.5	6	80000	90			0.5	1			±15	Vol. B
UA747	36	7	1.7	2.8	7.5	6	80000	90			0.5	2			±15	Vol. B
UA748	36	7	1.7	2.8	7.5	6	80000	90			0.5	2			±15	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

PRECISION OPERATIONAL AMPLIFIERS

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Page No.
	Max	Min	Typ	Max	Full Range	25°C										
TLC2652A	16	3.8	1.5	2.4	0.002	0.001	4	140	35	1.9	3.1	1			±5	Vol. A
TLC2652	16	3.8	1.5	2.4	0.004	0.003	4	140	23	1.9	3.1	1			±5	Vol. A
TLC2654A	16	4.6	1.5	2.4	0.024	0.01	50	125	20	1.9	3.7	1			±5	Vol. A
TLC2654	16	4.6	1.5	2.4	0.034	0.02	50	125	13	1.9	3.7	1			±5	Vol. A
TLE2027AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	13	2.8	1			±15	Vol. B
TLE2037AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	50	7.5	1			±15	Vol. B
TLC4501A	6	4	1	1.5	0.04	0.04	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4502A	6	4	1.25	3.5	0.05	0.05	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLC4501	6	4	1	1.5	0.08	0.08	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4502	6	4	1.25	3.5	0.1	0.1	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLE2027	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	13	2.8	1			±15	Vol. B
TLE2037	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	50	7.5	1			±15	Vol. B
LT1013A	44	4	0.35	0.5	0.24	0.15	−12000	117	22		0.4	2			±15	Vol. A
OP07C	36	6	2.7	5	0.25	0.15	±1800	120	9.8	0.6	0.3	1			±15	Vol. A
OP07D	36	6	2.7	5	0.25	0.15	±2000	110	9.8	0.6	0.3	1			±15	Vol. A
TLC2201A	16	4.6	1	1.5	0.3	0.2	1	110	15	1.8	2.5	1		RRO	5	Vol. A
TLC2201B	16	4.6	1	1.5	0.3	0.2	1	110	12	1.8	2.5	1		RRO	5	Vol. A
TLE2021B	40	4	0.2	0.3	0.3	0.2	25000	110	30	2	0.65	1			5	Vol. B
LT1013	44	4	0.35	0.55	0.4	0.3	−15000	114	22		0.4	2			±15	Vol. A
TLE2021A	40	4	0.2	0.3	0.6	0.3	25000	110	30	2	0.65	1			5	Vol. B
TLE2022B	40	4	0.225	0.3	0.4	0.3	33000	105	15	2.8	0.65	2			5	Vol. B
TLE2227	38	8	3.65	5.3	0.5	0.35	15000	115	2.5	13	2.5	2			±15	Vol. B
TLE2022A	40	4	0.225	0.3	0.55	0.4	33000	102	15	2.8	0.65	2			5	Vol. B
TLC1078	16	1.4	0.01	0.017	0.8	0.45	0.6	95	68	0.085	0.032	2			5	Vol. A
TLV2211	10	2.7	0.013	0.025	3	0.45	1	83	22	0.065	0.025	1		RRO	5	Vol. B
TLV2221	10	2.7	0.11	0.15	3	0.45	1	85	19	0.51	0.18	1		RRO	5	Vol. B
TLV2231	10	2.7	0.85	1.2	3	0.45	1	70	15	2	1.6	1		RRO	5	Vol. B
TLE2141A	44	4	3.5	4.5	0.8	0.5	−7000	108	10.5	5.9	45	1			±15	Vol. B
TLC277	16	3	0.7	1.6	1.5	0.5	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC27L7	16	3	0.01	0.017	2	0.5	0.6	94	68	0.085	0.03	2			5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

PRECISION OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Page No.
	Max	Min	Typ	Max	Full Range	25°C										
TLC27M7	16	3	0.105	0.28	2	0.5	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC2201	16	4.6	1	1.5	0.6	0.5	1	110	8	1.8	2.5	1		RRO	5	Vol. A
TLC2202A	16	4.6	0.85	1.3	0.65	0.5	1	100	15	1.9	2.5	2		RRO	5	Vol. A
TLC2202B	16	4.6	0.85	1.3	0.65	0.5	1	100	12	1.9	2.5	2		RRO	5	Vol. A
TLE2161B	36	7	0.29	0.35	1	0.5	4	90	40	6.4	10	1			±15	Vol. B
TLE2021	40	4	0.2	0.3	0.85	0.6	25000	110	15	2	0.65	1			5	Vol. B
TLE2022	40	4	0.225	0.3	0.8	0.6	35000	100	15	2.8	0.65	2			5	Vol. B
TLE2024B	40	4	0.2625	0.35	0.8	0.6	35000	95	15	2.8	0.7	4			5	Vol. B
TLE2142A	44	4	3.45	4.5	1.2	0.75	−7000	108	10.5	5.9	45	2			±15	Vol. B
TLC070A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1	Y		5	2–17
TLC071A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC072A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC073A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	2	Y		5	2–17
TLC074A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4			5	2–17
TLC075A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4	Y		5	2–17
TLC080A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1	Y		5	2–43
TLC081A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1			5	2–43
TLC082A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2			5	2–43
TLC083A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2	Y		5	2–43
TLC084A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4			5	2–43
TLC085A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4	Y		5	2–43
LT1013D	44	4	0.35	0.55	1	0.8	−15000	114	22		0.4	2			±15	Vol. A
TL031A	30	10	0.217	0.28	1.8	0.8	2	94	41	1.1	5.1	1			±15	Vol. A
TL032A	30	10	0.211	0.28	1.8	0.8	2	94	41	1.1	5.1	2			±15	Vol. A
TL051A	30	10	2.7	3.2	1.8	0.8	30	93	18	3.1	20	1			±15	Vol. A
TL052A	30	10	2.4	2.8	1.8	0.8	30	93	19	3	20.7	2			±15	Vol. A
TLC1079	16	1.4	0.01	0.017	1.2	0.85	0.6	95	68	0.085	0.032	4			5	Vol. A
TLC2252A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2254A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLV2252A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	2		RRO	5	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

Device	ΔV$_{CC}$ (V) Max	Min	I$_{CC}$ per channel (mA) Typ	Max	V$_{IO}$ (Max) (mV) Full Range	25°C	I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Page No.
TLV2254A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLE2024A	40	4	0.2625	0.35	1.05	0.85	40000	92	15	2.8	0.7	4			5	Vol. B
TLE2141	44	4	3.5	4.5	1.3	0.9	−7000	108	10.5	5.9	45	1			±15	Vol. B
TLC279	16	3	0.675	1.6	1.5	0.9	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC27L9	16	3	0.01	0.017	1.5	0.9	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27M9	16	3	0.105	0.28	1.5	0.9	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC2262A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2264A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2272A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	2		RRO	5	Vol. A
TLC2274A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	4		RRO	5	Vol. A
TLV2262A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2264A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2422A	10	2.7	0.05	0.075	1.5	0.95	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2432A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	2		RRO	5	Vol. B
TLV2434A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	4		RRO	5	Vol. B
TLV2442A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2444A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLC2202	16	4.6	0.85	1.3	1.15	1	1	100	8	1.9	2.5	2		RRO	5	Vol. A
TLC070	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1	Y		5	2–17
TLC071	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC072	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC073	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	2	Y		5	2–17
TLC074	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4			5	2–17
TLC075	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4	Y		5	2–17
TLC080	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1	Y		5	2–43
TLC081	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1			5	2–43
TLC082	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2			5	2–43
TLC083	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2	Y		5	2–43
TLC084	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4			5	2–43
TLC085	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4	Y		5	2–43

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIER
PRECISION SELECTION GUIDE

PRECISION OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Page No.
	Max	Min	Typ	Max	Full Range	25°C										
TLE2062B	36	7	0.3125	0.345	1.9	1	4	90	40	2	3.4	2			±15	Vol. B
TLV2450A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2451A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2452A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2453A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2454A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2455A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-NOISE OPERATIONAL AMPLIFIERS

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLE2027	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	13	2.8	1			± 15	Vol. B
TLE2027AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	13	2.8	1			± 15	Vol. B
TLE2037	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	50	7.5	1			± 15	Vol. B
TLE2037AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	50	7.5	1			± 15	Vol. B
TLE2227	38	8	3.65	5.3	0.5	0.35	15000	115	2.5	13	2.5	2			± 15	Vol. B
NE5534A	30	10	4	8	5	4	500000	100	3.5	10	13	1			±15	Vol. A
NE5534	30	10	4	8	5	4	500000	100	4	10	13	1			±15	Vol. A
NE5532	30	10	4	8	5	4	200000	100	5	10	9	2			±15	Vol. A
TLC070	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1	Y		5	2–17
TLC070A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1	Y		5	2–17
TLC071	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC071A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC072	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC072A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC073	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	2	Y		5	2–17
TLC073A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	2	Y		5	2–17
TLC074	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4			5	2–17
TLC074A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4			5	2–17
TLC075	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4	Y		5	2–17
TLC075A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4	Y		5	2–17
RC4136	30	10	1.25	2.825	7.5	6	140000	90	8	3	1.7	4			±15	Vol. A
RC4558	30	10	1.25	2.8	7.5	6	150000	90	8	3	1.7	2			±15	Vol. A
TLC2201	16	4.6	1	1.5	0.6	0.5	1	110	8	1.8	2.5	1		RRO	5	Vol. A
TLC2202	16	4.6	0.85	1.3	1.15	1	1	100	8	1.9	2.5	2		RRO	5	Vol. A
TLV2361	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	1			±2.5	Vol. B
TLV2362	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	2			±2.5	Vol. B
TLC080	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1	Y		5	2–43
TLC080A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1	Y		5	2–43
TLC081	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1			5	2–43
TLC081A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1			5	2–43
TLC082	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2			5	2–43
TLC082A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2			5	2–43

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-NOISE OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLC083	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2	Y		5	2–43
TLC083A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2	Y		5	2–43
TLC084	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4			5	2–43
TLC084A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4			5	2–43
TLC085	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4	Y		5	2–43
TLC085A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4	Y		5	2–43
TLC2272	16	4.4	1.1	1.5	3	2.5	1	75	9	2.18	3.6	2		RRO	5	Vol. A
TLC2272A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	2		RRO	5	Vol. A
TLC2274	16	4.4	1.1	1.5	3	2.5	1	75	9	2.18	3.6	4		RRO	5	Vol. A
TLC2274A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	4		RRO	5	Vol. A
OP07C	36	6	2.7	5	0.25	0.15	±1800	120	9.8	0.6	0.3	1			±15	Vol. A
OP07D	36	6	2.7	5	0.25	0.15	±2000	110	9.8	0.6	0.3	1			±15	Vol. A
TLE2141	44	4	3.5	4.5	1.3	0.9	−7000	108	10.5	5.9	45	1			± 15	Vol. B
TLE2141A	44	4	3.5	4.5	0.8	0.5	−7000	108	10.5	5.9	45	1			± 15	Vol. B
TLE2142	44	4	3.45	4.5	1.6	1.2	−7000	108	10.5	5.9	45	2			± 15	Vol. B
TLE2142A	44	4	3.45	4.5	1.2	0.75	−7000	108	10.5	5.9	45	2			± 15	Vol. B
TLE2144	44	4	3.45	4.5	3.2	2.4	−7000	108	10.5	5.9	45	4			± 15	Vol. B
TLE2144A	44	4	3.45	4.5	2.4	1.5	−7000	108	10.5	5.9	45	4			± 15	Vol. B
TLV2460	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2460A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2461	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2461A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2462	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2462A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2463	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2463A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2464	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2464A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2465	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2465A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLC2201B	16	4.6	1	1.5	0.3	0.2	1	110	12	1.8	2.5	1		RRO	5	Vol. A
TLC2202B	16	4.6	0.85	1.3	0.65	0.5	1	100	12	1.9	2.5	2		RRO	5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-NOISE OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLC2262	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2262A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2264	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2264A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC4501	6	4	1	1.5	0.08	0.08	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4501A	6	4	1	1.5	0.04	0.04	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4502	6	4	1.25	3.5	0.1	0.1	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLC4502A	6	4	1.25	3.5	0.05	0.05	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLV2262	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2262A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2264	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2264A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLC2654	16	4.6	1.5	2.4	0.034	0.02	50	125	13	1.9	3.7	1			± 5	Vol. A
TLE2071	38	4.5	1.7	2.2	6	4	20	98	14	10	45	1			± 15	Vol. B
TLE2071A	38	4.5	1.7	2.2	4	2	20	98	14	10	45	1			± 15	Vol. B
TLE2072	38	4.5	1.55	1.8	7.8	6	20	98	14	10	45	2			± 15	Vol. B
TLE2072A	38	4.5	1.55	1.8	5.3	3.5	20	98	14	10	45	2			± 15	Vol. B
TLE2074	38	4.5	1.425	1.875	7.1	5	25	98	14	10	45	4			± 15	Vol. B
TLE2074A	38	4.5	1.425	1.875	5.1	3	25	98	14	10	45	4			± 15	Vol. B
TLE2081	38	4.5	1.7	2.2	8	6	20	98	14	10	45	1			± 15	Vol. B
TLE2081A	38	4.5	1.7	2.2	5	3	20	98	14	10	45	1			± 15	Vol. B
TLE2082	38	4.5	1.55	1.8	8.1	7	20	98	14	10	45	2			± 15	Vol. B
TLE2082A	38	4.5	1.55	1.8	5.1	4	20	98	14	10	45	2			± 15	Vol. B
TLE2084	38	4.5	1.625	1.875	9.1	7	25	98	14	10	45	4			± 15	Vol. B
TLE2084A	38	4.5	1.625	1.875	6.1	4	25	98	14	10	45	4			± 15	Vol. B
TLC2201A	16	4.6	1	1.5	0.3	0.2	1	110	15	1.8	2.5	1		RRO	5	Vol. A
TLC2202A	16	4.6	0.85	1.3	0.65	0.5	1	100	15	1.9	2.5	1		RRO	5	Vol. A
TLE2021	40	4	0.2	0.3	0.85	0.6	25000	110	15	2	0.65	1			5	Vol. B
TLE2022	40	4	0.225	0.3	0.8	0.6	35000	100	15	2.8	0.65	2			5	Vol. B
TLE2022A	40	4	0.225	0.3	0.55	0.4	33000	102	15	2.8	0.65	2			5	Vol. B
TLE2022B	40	4	0.225	0.3	0.4	0.3	33000	105	15	2.8	0.65	2			5	Vol. B
TLE2024	40	4	0.2625	0.35	1.3	1.1	46000	90	15	2.8	0.7	4			5	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

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OPERATIONAL AMPLIFIER
LOW-NOISE SELECTION GUIDE

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LOW-NOISE OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLE2024A	40	4	0.2625	0.35	1.05	0.85	40000	92	15	2.8	0.7	4			5	Vol. B
TLE2024B	40	4	0.2625	0.35	0.8	0.6	35000	95	15	2.8	0.7	4			5	Vol. B
TLV2231	10	2.7	0.85	1.2	3	0.45	1	70	15	2	1.6	1		RRO	5	Vol. B
TLV2470	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2470A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1		RRIO	3	2–153
TLV2472	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2472A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2473	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2473A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2474	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2474A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2475	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2475A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2731	10	2.7	0.75	1.2	0.75	3	1	70	16	2	1.25	1		RRO	3	2–229
LF347	36	7	2	2.75	13	10	50	100	18	3	13	4			±15	Vol. A
LF347B	36	7	2	2.75	7	5	50	100	18	3	13	4			±15	Vol. A
LF353	36	7	1.8	3.25	13	10	50	100	18	3	13	2			±15	Vol. A
LF411	36	7	2	3.4		2	50	100	18	3	13	1			±15	Vol. A
LF412	36	7	2.25	3.4		3	50	100	18	3	13	2			±15	Vol. A
TL051	30	10	2.7	3.2	2.5	1.5	30	93	18	3.1	20	1			±15	Vol. A
TL051A	30	10	2.7	3.2	1.8	0.8	30	93	18	3.1	20	1			±15	Vol. A
TL070	36	7	1.4	2.5	13	10	65	100	18	3	13	1			±15	Vol. A
TL071	36	7	1.4	2.5	13	10	65	100	18	3	13	1			±15	Vol. A
TL071A	36	7	1.4	2.5	7.5	6	65	100	18	3	13	1			±15	Vol. A
TL071B	36	7	1.4	2.5	5	3	65	100	18	3	13	1			±15	Vol. A
TL072	36	7	1.4	2.5	13	10	65	100	18	3	13	2			±15	Vol. A
TL072A	36	7	1.4	2.5	7.5	6	65	100	18	3	13	2			±15	Vol. A
TL072B	36	7	1.4	2.5	5	3	65	100	18	3	13	2			±15	Vol. A
TL074	36	7	1.4	2.5	13	10	65	100	18	3	13	4			±15	Vol. A
TL074A	36	7	1.4	2.5	7.5	6	65	100	18	3	13	4			±15	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-NOISE OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TL074B	36	7	1.4	2.5	5	3	65	100	18	3	13	4			±15	Vol. A
TL081	36	7	1.4	2.8	20	15	30	86	18	3	13	1			±15	Vol. A
TL081A	36	7	1.4	2.8	7.5	6	30	86	18	3	13	1			±15	Vol. A
TL081B	36	7	1.4	2.8	5	3	30	86	18	3	13	1			±15	Vol. A
TL082	36	7	1.4	2.8	20	15	30	86	18	3	13	2			±15	Vol. A
TL082A	36	7	1.4	2.8	7.5	6	30	86	18	3	13	2			±15	Vol. A
TL082B	36	7	1.4	2.8	5	3	30	86	18	3	13	2			±15	Vol. A
TL084	36	7	1.4	2.8	20	15	30	86	18	3	13	4			±15	Vol. A
TL084A	36	7	1.4	2.8	7.5	6	30	86	18	3	13	4			±15	Vol. A
TL084B	36	7	1.4	2.8	5	3	30	86	18	3	13	4			±15	Vol. A
TLV2422	10	2.7	0.05	0.075	2.5	2	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2422A	10	2.7	0.05	0.075	1.5	0.95	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2432	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	2		RRO	5	Vol. B
TLV2432A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	2		RRO	5	Vol. B
TLV2434	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	4		RRO	5	Vol. B
TLV2434A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	4		RRO	5	Vol. B
TLV2442	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2442A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2444	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2444A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TL052	30	10	2.4	2.8	2.5	1.5	30	93	19	3	20.7	2			±15	Vol. A
TL052A	30	10	2.4	2.8	1.8	0.8	30	93	19	3	20.7	2			±15	Vol. A
TLC2252	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2252A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2254	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLC2254A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLV2221	10	2.7	0.11	0.15	3	0.45	1	85	19	0.51	0.18	1		RRO	5	Vol. B
TLV2252	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2252A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2254	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2254A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLC2654A	16	4.6	1.5	2.4	0.024	0.01	50	125	20	1.9	3.7	1			±5	Vol. B
TLV2721	10	2.7	0.11	0.15	0.6	3	1	82	20	0.51	0.18	1		RRO	3	2–203

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIER
LOW-NOISE SELECTION GUIDE

LOW-POWER OPERATIONAL AMPLIFIERS

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) $(nV/\sqrt{Hz})$	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2324	8	2	0.01	0.017	12	10	0.6	94	68	0.027	0.02	4			5	Vol. B
TLV2322	8	2	0.01	0.017	11	9	0.6	94	68	0.027	0.02	2			5	Vol. B
TLC27L9	16	3	0.01	0.017	1.5	0.9	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L7	16	3	0.01	0.017	2	0.5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L4B	16	3	0.01	0.017	3	2	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L4A	16	3	0.01	0.017	6.5	5	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L4	16	3	0.01	0.017	12	10	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L2B	16	3	0.01	0.017	3.5	2	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L2A	16	3	0.01	0.017	7	5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L2	16	3	0.01	0.017	13	10	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L1B	16	3	0.01	0.017	3.5	2	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC27L1A	16	3	0.01	0.017	7	5	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC27L1	16	3	0.01	0.017	13	10	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC25L4B	16	1.4	0.01	0.017	3	2	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4A	16	1.4	0.01	0.017	6.5	5	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4	16	1.4	0.01	0.017	12	10	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L2B	16	1.4	0.01	0.017	3	2	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2A	16	1.4	0.01	0.017	6.5	5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2	16	1.4	0.01	0.017	12	10	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC1079	16	1.4	0.01	0.017	1.2	0.85	0.6	95	68	0.085	0.032	4			5	Vol. A
TLC1078	16	1.4	0.01	0.017	0.8	0.45	0.6	95	68	0.085	0.032	2			5	Vol. A
TLV2711	10	2.7	0.013	0.025	0.47	3	1	83	22	0.065	0.025	1		RRO	3	2–177
TLV2211	10	2.7	0.013	0.025	3	0.45	1	83	22	0.065	0.025	1		RRO	5	Vol. B
TLV2455A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2455	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2454A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2454	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2453A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2453	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2452A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2452	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2451A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1		RRIO	3	2–99

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2451	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2450A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2450	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2254A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2254	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2252A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2252	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLC2254A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLC2254	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLC2252A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2252	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLV2422A	10	2.7	0.05	0.075	1.5	0.95	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2422	10	2.7	0.05	0.075	2.5	2	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2432A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	2		RRO	5	Vol. B
TLV2432	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	2		RRO	5	Vol. B
TLV2434A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	4		RRO	5	Vol. B
TLV2434	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	4		RRO	5	Vol. B
TL022	30	10	0.065	0.125	7.5	5	100000	72	50	0.5	0.5	2			±15	Vol. A
TLV2721	10	2.7	0.11	0.15	0.6	3	1	82	20	0.51	0.18	1		RRO	3	2–203
TLV2221	10	2.7	0.11	0.15	3	0.45	1	85	19	0.51	0.18	1		RRO	5	Vol. B
TLV2264A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2264	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2262A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2262	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLC2264A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2264	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2262A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2262	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TL064B	36	7	0.2	0.25	5	3	30	86	42	1	3.5	4			±15	Vol. A
TL064A	36	7	0.2	0.25	7.5	6	30	86	42	1	3.5	4			±15	Vol. A
TL064	36	7	0.2	0.25	20	15	30	86	42	1	3.5	4			±15	Vol. A
TL062B	36	7	0.2	0.25	5	3	30	86	42	1	3.5	2			±15	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIER
LOW-POWER SELECTION GUIDE

LOW-POWER OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TL062A	36	7	0.2	0.25	7.5	6	30	86	42	1	3.5	2			±15	Vol. A
TL062	36	7	0.2	0.25	20	15	30	86	42	1	3.5	2			±15	Vol. A
TL061B	36	7	0.2	0.25	5	3	30	86	42	1	3.5	1			±15	Vol. A
TL061A	36	7	0.2	0.25	7.5	6	30	86	42	1	3.5	1			±15	Vol. A
TL061	36	7	0.2	0.25	20	15	30	86	42	1	3.5	1			±15	Vol. A
TLV2334	8	2	0.1	0.28	12	10	0.6	91	32	0.3	0.38	4			5	Vol. B
TLV2332	8	2	0.1	0.28	11	9	0.6	91	32	0.3	0.38	2			5	Vol. B
TLC27M9	16	3	0.105	0.28	1.5	0.9	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC27M7	16	3	0.105	0.28	2	0.5	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC27M4B	16	3	0.105	0.28	3	2	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC27M4A	16	3	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC27M4	16	3	0.105	0.28	12	10	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC27M2B	16	3	0.105	0.28	3.5	2	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC27M2A	16	3	0.105	0.28	7	5	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC27M2	16	3	0.105	0.28	13	10	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC25M4B	16	1.4	0.105	0.28	3	2	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC25M4A	16	1.4	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC25M4	16	1.4	0.105	0.28	12	10	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC25M2A	16	1.4	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC25M2	16	1.4	0.105	0.28	12	10	0.6	91	32	0.525	0.43	2			5	Vol. A
TL034A	30	10	0.2175	0.28	3.7	1.5	2	94	43	1.1	5.1	4			±15	Vol. A
TL034	30	10	0.2175	0.28	6.2	4	2	94	43	1.1	5.1	4			±15	Vol. A
TL032A	30	10	0.211	0.28	1.8	0.8	2	94	41	1.1	5.1	2			±15	Vol. A
TL032	30	10	0.211	0.28	2.5	1.5	2	94	41	1.1	5.1	2			±15	Vol. A
TL031A	30	10	0.217	0.28	1.8	0.8	2	94	41	1.1	5.1	1			±15	Vol. A
TL031	30	10	0.217	0.28	2.5	1.5	2	94	41	1.1	5.1	1			±15	Vol. A
TLE2022B	40	4	0.225	0.3	0.4	0.3	33000	105	15	2.8	0.65	2			5	Vol. B
TLE2022A	40	4	0.225	0.3	0.55	0.4	33000	102	15	2.8	0.65	2			5	Vol. B
TLE2022	40	4	0.225	0.3	0.8	0.6	35000	100	15	2.8	0.65	2			5	Vol. B
TLE2021B	40	4	0.2	0.3	0.3	0.2	25000	110	30	2	0.65	1			5	Vol. B
TLE2021A	40	4	0.2	0.3	0.6	0.3	25000	110	30	2	0.65	1			5	Vol. B
TLE2021	40	4	0.2	0.3	0.85	0.6	25000	110	15	2	0.65	1			5	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-POWER OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V) Max	Min	I$_{CC}$ per channel (mA) Typ	Max	V$_{IO}$ (Max) (mV) Full Range	25°C	I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
LM324A	32	3	0.175	0.3	5	3	−15000	80	23	0.4	0.25	4			5	Vol. A
LM324	32	3	0.175	0.3	9	7	−20000	80	23	0.4	0.25	4			5	Vol. A
LM2902	26	3	0.175	0.3	10	7	−20000	80	23	0.4	0.25	4			5	Vol. A
TLE2062B	36	7	0.31	0.345	1.9	1	4	90	40	2	3.4	2			±15	Vol. B
TLE2062A	36	7	0.31	0.345	2.9	2	4	90	40	2	3.4	2			±15	Vol. B
TLE2062	36	7	0.31	0.345	4.9	4	4	90	40	2	3.4	2			±15	Vol. B
TLE2161B	36	7	0.29	0.35	1	0.5	4	90	40	6.4	10	1			±15	Vol. B
TLE2161A	36	7	0.29	0.35	2.5	1.5	4	90	40	6.4	10	1			±15	Vol. B
TLE2161	36	7	0.29	0.35	3.9	3	4	90	40	6.4	10	1			±15	Vol. B
TLE2064B	36	7	0.31	0.35	2.9	2	4	90	40	2	3.4	4			±15	Vol. B
TLE2064A	36	7	0.31	0.35	4.9	4	4	90	40	2	3.4	4			±15	Vol. B
TLE2064	36	7	0.31	0.35	6.9	6	4	90	40	2	3.4	4			±15	Vol. B
TLE2061B	36	7	0.29	0.35	2.4	1.9	4	90	40	2	3.4	1			±15	Vol. B
TLE2061A	36	7	0.29	0.35	3.5	2.6	4	90	40	2	3.4	1			±15	Vol. B
TLE2061	36	7	0.29	0.35	4	3	4	90	40	2	3.4	1			±15	Vol. B
TLE2024B	40	4	0.26	0.35	0.8	0.6	35000	95	15	2.8	0.7	4			5	Vol. B
TLE2024A	40	4	0.26	0.35	1.05	0.85	40000	92	15	2.8	0.7	4			5	Vol. B
TLE2024	40	4	0.26	0.35	1.3	1.1	46000	90	15	2.8	0.7	4			5	Vol. B
LT1013A	44	4	0.35	0.5	0.24	0.15	−12000	117	22		0.4	2			±15	Vol. A
LT1013D	44	4	0.35	0.55	1	0.8	−15000	114	22		0.4	2			±15	Vol. A
LT1013	44	4	0.35	0.55	0.4	0.3	−15000	114	22		0.4	2			±15	Vol. A
TLV2465A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2465	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2464A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2464	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2463A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2463	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2462A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2462	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2461A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2461	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2460A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-POWER OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2460	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
LM2904	26	3	0.35	0.6	10	7	–20000	80	23	0.4	0.15	2			5	Vol. A
TLV2442A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2444A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLV2475A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2475	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2474A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2474	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2473A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2473	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2472A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2472	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2471A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1		RRIO	3	2–153
TLV2471	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2470A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2470	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
LM358A	32	3	0.5	1	5	3	–15000	80	23	0.4		2			5	Vol. A
LM358	32	3	0.5	1	9	7	–20000	80	23	0.4		2			5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/$\sqrt{Hz}$)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Page No.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2324	8	2	0.01	0.017	12	10	0.6	94	68	0.027	0.02	4			5	Vol. B
TLV2322	8	2	0.01	0.017	11	9	0.6	94	68	0.027	0.02	2			5	Vol. B
TLC27L9	16	3	0.01	0.017	1.5	0.9	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L7	16	3	0.01	0.017	2	0.5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L4B	16	3	0.01	0.017	3	2	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L4A	16	3	0.01	0.017	6.5	5	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L4	16	3	0.01	0.017	12	10	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC27L2B	16	3	0.01	0.017	3.5	2	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L2A	16	3	0.01	0.017	7	5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L2	16	3	0.01	0.017	13	10	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC27L1B	16	3	0.01	0.017	3.5	2	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC27L1A	16	3	0.01	0.017	7	5	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC27L1	16	3	0.01	0.017	13	10	0.6	94	68	0.085	0.03	1			5	Vol. A
TLC25L4B	16	1.4	0.01	0.017	3	2	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4A	16	1.4	0.01	0.017	6.5	5	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4	16	1.4	0.01	0.017	12	10	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L2B	16	1.4	0.01	0.017	3	2	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2A	16	1.4	0.01	0.017	6.5	5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2	16	1.4	0.01	0.017	12	10	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC1079	16	1.4	0.01	0.017	1.2	0.85	0.6	95	68	0.085	0.032	4			5	Vol. A
TLC1078	16	1.4	0.01	0.017	0.8	0.45	0.6	95	68	0.085	0.032	2			5	Vol. A
TLV2711	10	2.7	0.013	0.025	0.47	3	1	83	22	0.065	0.025	1		RRO	3	2–177
TLV2211	10	2.7	0.013	0.025	3	0.45	1	83	22	0.065	0.025	1		RRO	5	Vol. B
TLV2455A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2455	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2454A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2454	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2453A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2453	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2452A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2452	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2451A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1		RRIO	3	2–99

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIER
MICRO-POWER SELECTION GUIDE

MICROPOWER OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Page No.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2451	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2450A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2450	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2254A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2254	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2252A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2252	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLC2254A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	4		RRO	5	Vol. B
TLC2254	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	4		RRO	5	Vol. B
TLC2252A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	2		RRO	5	Vol. B
TLC2252	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	2		RRO	5	Vol. B
TLV2422A	10	2.7	0.05	0.075	1.5	0.95	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2422	10	2.7	0.05	0.075	2.5	2	1	90	18	0.052	0.02	2		RRO	5	2–69

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-VOLTAGE OPERATIONAL AMPLIFIERS

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2361	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	1			±2.5	Vol. B
TLV2362	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	2			±2.5	Vol. B
TLV2770	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2770A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2771	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1		RRO	2.7	2–255
TLV2771A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1		RRO	2.7	2–255
TLV2772	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2772A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2773	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2	Y	RRO	2.7	2–255
TLV2773A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2	Y	RRO	2.7	2–255
TLV2774	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4		RRO	2.7	2–255
TLV2774A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4		RRO	2.7	2–255
TLV2775	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4	Y	RRO	2.7	2–255
TLV2775A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4	Y	RRO	2.7	2–255
TLV2450	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2450A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2451	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2451A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2452	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2452A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2453	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2453A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2454	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2454A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2455	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2455A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2460	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2460A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2461	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2461A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1		RRIO	3	2–127

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

LOW-VOLTAGE OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2462	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2462A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2463	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2463A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2464	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2464A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2465	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2465A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2470	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2470A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1		RRIO	3	2–153
TLV2472	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2472A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2473	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2473A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2474	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2474A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2475	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2475A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2322	8	2	0.01	0.017	11	9	0.6	94	68	0.027	0.02	2			5	Vol. B
TLV2324	8	2	0.01	0.017	12	10	0.6	94	68	0.027	0.02	4			5	Vol. B
TLV2332	8	2	0.1	0.28	11	9	0.6	91	32	0.3	0.38	2			5	Vol. B
TLV2334	8	2	0.1	0.28	12	10	0.6	91	32	0.3	0.38	4			5	Vol. B
TLV2341	8	2	0.675	1.6	10	8	0.6	80	25	1.7	3.6	1			5	Vol. B
TLV2342	8	2	0.325	1.5	11	9	0.6	80	25	0.79	2.1	2			5	Vol. B
TLV2344	8	2	0.325	1.5	12	10	0.6	78	25	0.79	2.1	4			5	Vol. B
TLV2252	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2252A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2254	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	4		RRO	5	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

Device	ΔV$_{CC}$ (V) Max	Min	I$_{CC}$ per channel (mA) Typ	Max	V$_{IO}$ (Max) (mV) Full Range	25°C	I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
TLV2254A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2262	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2262A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2264	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2264A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2211	10	2.7	0.013	0.025	3	0.45	1	83	22	0.065	0.025	1		RRO	5	Vol. B
TLV2221	10	2.7	0.11	0.15	3	0.45	1	85	19	0.51	0.18	1		RRO	5	Vol. B
TLV2231	10	2.7	0.85	1.2	3	0.45	1	70	15	2	1.6	1		RRO	5	Vol. B
TLV2422	10	2.7	0.05	0.075	2.5	2	1	90	18	0.052	0.02	2		RRO	5	2–71
TLV2422A	10	2.7	0.05	0.075	1.5	0.95	1	90	18	0.052	0.02	2		RRO	5	2–71
TLV2432	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	2		RRO	5	Vol. B
TLV2432A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	2		RRO	5	Vol. B
TLV2434	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	4		RRO	5	Vol. B
TLV2434A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	4		RRO	5	Vol. B
TLV2442	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2442A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2444	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLV2444A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLV2711	10	2.7	0.013	0.025	0.47	3	1	83	22	0.065	0.025	1		RRO	3	2–183
TLV2721	10	2.7	0.11	0.15	0.6	3	1	82	20	0.51	0.18	1		RRO	3	2–209
TLV2731	10	2.7	0.75	1.2	0.75	3	1	70	16	2	1.25	1		RRO	3	2–235
TLC1078	16	1.4	0.01	0.017	0.8	0.45	0.6	95	68	0.085	0.032	2			5	Vol. A
TLC1079	16	1.4	0.01	0.017	1.2	0.85	0.6	95	68	0.085	0.032	4			5	Vol. A
TLC251	16	1.4	0.675	1.6	12	10	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC251A	16	1.4	0.675	1.6	6.5	5	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC251B	16	1.4	0.675	1.6	3	2	0.6	80	25	1.7	3.6	1			5	Vol. A
TLC252	16	1.4	0.7	1.6	12	10	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC252A	16	1.4	0.7	1.6	6.5	5	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC252B	16	1.4	0.7	1.6	3	2	0.6	80	25	1.7	3.6	2			5	Vol. A
TLC254	16	1.4	0.775	1.8	12	10	0.6	80	25	1.7	3.6	1			5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

TEXAS INSTRUMENTS
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OPERATIONAL AMPLIFIER
LOW-VOLTAGE SELECTION GUIDE

LOW-VOLTAGE OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLC254A	16	1.4	0.775	1.8	6.5	5	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC254B	16	1.4	0.775	1.8	3	2	0.6	80	25	1.7	3.6	4			5	Vol. A
TLC25L2	16	1.4	0.01	0.017	12	10	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2A	16	1.4	0.01	0.017	6.5	5	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L2B	16	1.4	0.01	0.017	3	2	0.6	94	68	0.085	0.03	2			5	Vol. A
TLC25L4	16	1.4	0.01	0.017	12	10	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4A	16	1.4	0.01	0.017	6.5	5	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25L4B	16	1.4	0.01	0.017	3	2	0.6	94	70	0.085	0.03	4			5	Vol. A
TLC25M2	16	1.4	0.105	0.28	12	10	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC25M2A	16	1.4	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	2			5	Vol. A
TLC25M4	16	1.4	0.105	0.28	12	10	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC25M4A	16	1.4	0.105	0.28	6.5	5	0.6	91	32	0.525	0.43	4			5	Vol. A
TLC25M4B	16	1.4	0.105	0.28	3	2	0.6	91	32	0.525	0.43	4			5	Vol. A

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

TEXAS
INSTRUMENTS

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2450	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2450A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1	Y	RRIO	3	2–99
TLV2451	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2451A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	1		RRIO	3	2–99
TLV2452	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2452A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2		RRIO	3	2–99
TLV2453	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2453A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	2	Y	RRIO	3	2–99
TLV2454	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2454A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4		RRIO	3	2–99
TLV2455	6	2.7	0.023	0.035	2	1.5	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2455A	6	2.7	0.023	0.035	1.3	1	900	86	51	0.22	0.12	4	Y	RRIO	3	2–99
TLV2460	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2460A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2461	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2461A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2462	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2462A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2463	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2463A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2464	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2464A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2465	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2465A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2470	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2470A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	1	Y	RRIO	3	2–153
TLV2471A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	1		RRIO	3	2–153
TLV2472	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2		RRIO	3	2–153
TLV2472A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2		RRIO	3	2–153

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIER
RAIL-TO-RAIL SELECTION GUIDE

RAIL-TO-RAIL OPERATIONAL AMPLIFIERS (continued)

Device	ΔV$_{CC}$ (V)		I$_{CC}$ per channel (mA)		V$_{IO}$ (Max) (mV)		I$_{IB}$ (Typ) (pA)	CMRR (Typ) (dB)	V$_n$ @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V$_{CC}$ (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2473	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2473A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	2	Y	RRIO	3	2–153
TLV2474	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2474A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4		RRIO	3	2–153
TLV2475	6	2.7	0.55	0.75	2.4	2.2	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLV2475A	6	2.7	0.55	0.75	1.8	1.6	2	78	15	2.8	1.4	4	Y	RRIO	3	2–153
TLC2201	16	4.6	1	1.5	0.6	0.5	1	110	8	1.8	2.5	1		RRO	5	Vol. A
TLC2201A	16	4.6	1	1.5	0.3	0.2	1	110	15	1.8	2.5	1		RRO	5	Vol. A
TLC2201B	16	4.6	1	1.5	0.3	0.2	1	110	12	1.8	2.5	1		RRO	5	Vol. A
TLC2202	16	4.6	0.85	1.3	1.15	1	1	100	8	1.9	2.5	2		RRO	5	Vol. A
TLC2202A	16	4.6	0.85	1.3	0.65	0.5	1	100	15	1.9	2.5	2		RRO	5	Vol. A
TLC2202B	16	4.6	0.85	1.3	0.65	0.5	1	100	12	1.9	2.5	2		RRO	5	Vol. A
TLC2252	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2252A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	2		RRO	5	Vol. A
TLC2254	16	4.4	0.035	0.0625	1.75	1.5	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLC2254A	16	4.4	0.035	0.0625	1	0.85	1	83	19	0.2	0.12	4		RRO	5	Vol. A
TLC2262	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2262A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	2		RRO	5	Vol. A
TLC2264	16	4.4	0.2	0.25	3	2.5	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2264A	16	4.4	0.2	0.25	1.5	0.95	1	83	12	0.82	0.55	4		RRO	5	Vol. A
TLC2272	16	4.4	1.1	1.5	3	2.5	1	75	9	2.18	3.6	2		RRO	5	Vol. A
TLC2272A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	2		RRO	5	Vol. A
TLC2274	16	4.4	1.1	1.5	3	2.5	1	75	9	2.18	3.6	4		RRO	5	Vol. A
TLC2274A	16	4.4	1.1	1.5	1.5	0.95	1	75	9	2.18	3.6	4		RRO	5	Vol. A
TLC4501	6	4	1	1.5	0.08	0.08	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4501A	6	4	1	1.5	0.04	0.04	1	100	12	4.7	2.5	1		RRO	5	Vol. A
TLC4502	6	4	1.25	3.5	0.1	0.1	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLC4502A	6	4	1.25	3.5	0.05	0.05	1	100	12	4.7	2.5	2		RRO	5	Vol. A
TLV2211	10	2.7	0.013	0.025	3	0.45	1	83	22	0.065	0.025	1		RRO	5	Vol. B
TLV2221	10	2.7	0.11	0.15	3	0.45	1	85	19	0.51	0.18	1		RRO	5	Vol. B

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

RAIL-TO-RAIL OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_CC (V)		I_CC per channel (mA)		V_IO (Max) (mV)		I_IB (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_CC (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2231	10	2.7	0.85	1.2	3	0.45	1	70	15	2	1.6	1		RRO	5	Vol. B
TLV2252	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2252A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	2		RRO	5	Vol. B
TLV2254	8	2.7	0.034	0.0625	1.75	1.5	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2254A	8	2.7	0.034	0.0625	1	0.85	1	75	19	0.187	0.1	4		RRO	5	Vol. B
TLV2262	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2262A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	2		RRO	5	Vol. B
TLV2264	8	2.7	0.2	0.25	3	2.5	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2264A	8	2.7	0.2	0.25	1.5	0.95	1	83	12	0.67	0.55	4		RRO	5	Vol. B
TLV2422	10	2.7	0.05	0.075	2.5	2	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2422A	10	2.7	0.05	0.075	1.5	0.95	1	90	18	0.052	0.02	2		RRO	5	2–69
TLV2432	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	2		RRO	5	Vol. B
TLV2432A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	2		RRO	5	Vol. B
TLV2434	10	2.7	0.098	0.125	2.5	2	1	90	18	0.5	0.25	4		RRO	5	Vol. B
TLV2434A	10	2.7	0.098	0.125	1.5	0.95	1	83	18	0.5	0.25	4		RRO	5	Vol. B
TLV2442	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2444A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLV2444	10	2.7	0.75	1.1	2.5	2	1	75	18	1.75	1.3	4		RRO	5	Vol. B
TLV2442A	10	2.7	1.1	0.725	1.5	0.95	1	75	18	1.75	1.3	2		RRO	5	Vol. B
TLV2711	10	2.7	0.013	0.025	0.47	3	1	83	22	0.065	0.025	1		RRO	3	2–177
TLV2721	10	2.7	0.11	0.15	0.6	3	1	82	20	0.51	0.18	1		RRO	3	2–203
TLV2731	10	2.7	0.75	1.2	0.75	3	1	70	16	2	1.25	1		RRO	3	2–229
TLV2770	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2770A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2771	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1		RRO	2.7	2–255
TLV2771A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1		RRO	2.7	2–255
TLV2772	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2772A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2773	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2	Y	RRO	2.7	2–255
TLV2773A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2	Y	RRO	2.7	2–255

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

OPERATIONAL AMPLIFIER
RAIL-TO-RAIL SELECTION GUIDE

RAIL-TO-RAIL OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2774	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4		RRO	2.7	2–261
TLV2774A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4		RRO	2.7	2–261
TLV2775	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4	Y	RRO	2.7	2–261
TLV2775A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4	Y	RRO	2.7	2–261

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/µs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLE2037	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	50	7.5	1			±15	Vol. B
TLE2037AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	50	7.5	1			±15	Vol. B
LM318	40	10	5	10	15	10	150000	100	23	15	70	1			±15	Vol. A
TLE2027	38	8	3.8	5.3	0.145	0.1	15000	131	2.5	13	2.8	1			±15	Vol. B
TLE2027AM	38	8	3.8	5.3	0.1	0.025	15000	131	2.5	13	2.8	1			±15	Vol. B
TLE2227	38	8	3.65	5.3	0.5	0.35	15000	115	2.5	13	2.5	2			±15	Vol. B
TLE2071	38	4.5	1.7	2.2	6	4	20	98	14	10	45	1			±15	Vol. B
TLE2071A	38	4.5	1.7	2.2	4	2	20	98	14	10	45	1			±15	Vol. B
TLE2072	38	4.5	1.55	1.8	7.8	6	20	98	14	10	45	2			±15	Vol. B
TLE2072A	38	4.5	1.55	1.8	5.3	3.5	20	98	14	10	45	2			±15	Vol. B
TLE2074	38	4.5	1.425	1.875	7.1	5	25	98	14	10	45	4			±15	Vol. B
TLE2074A	38	4.5	1.425	1.875	5.1	3	25	98	14	10	45	4			±15	Vol. B
TLE2081	38	4.5	1.7	2.2	8	6	20	98	14	10	45	1			±15	Vol. B
TLE2081A	38	4.5	1.7	2.2	5	3	20	98	14	10	45	1			±15	Vol. B
TLE2082	38	4.5	1.55	1.8	8.1	7	20	98	14	10	45	2			±15	Vol. B
TLE2082A	38	4.5	1.55	1.8	5.1	4	20	98	14	10	45	2			±15	Vol. B
TLE2084	38	4.5	1.625	1.875	9.1	7	25	98	14	10	45	4			±15	Vol. B
TLE2084A	38	4.5	1.625	1.875	6.1	4	25	98	14	10	45	4			±15	Vol. B
TLC070	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1	Y		5	2–17
TLC070A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1	Y		5	2–17
TLC071	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC071A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC072	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	1			5	2–17
TLC072A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	1			5	2–17
TLC073	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	2	Y		5	2–17
TLC073A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	2	Y		5	2–17
TLC074	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4			5	2–17
TLC074A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4			5	2–17
TLC075	16	4.5	1.9	2.5	1.5	1	1.5	140	7	10	16	4	Y		5	2–17
TLC075A	16	4.5	1.9	2.5	1	0.75	1.5	140	7	10	16	4	Y		5	2–17

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

WIDE-BANDWIDTH (HIGHER-SPEED) OPERATIONAL AMPLIFIERS (continued)

Device	ΔV_CC (V)		I_CC per channel (mA)		V_IO (Max) (mV)		I_IB (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_CC (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLC080	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1	Y		5	2–43
TLC080A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1	Y		5	2–43
TLC081	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	1			5	2–43
TLC081A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	1			5	2–43
TLC082	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2			5	2–43
TLC082A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2			5	2–43
TLC083	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	2	Y		5	2–43
TLC083A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	2	Y		5	2–43
TLC084	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4			5	2–43
TLC084A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4			5	2–43
TLC085	16	4.5	1.9	2.5	1.5	1	3	140	8.5	10	16	4	Y		5	2–43
TLC085A	16	4.5	1.9	2.5	1	0.75	3	140	8.5	10	16	4	Y		5	2–43
NE5534	30	10	4	8	5	4	500000	100	4	10	13	1			±15	Vol. A
NE5534A	30	10	4	8	5	4	500000	100	3.5	10	13	1			±15	Vol. A
NE5532	30	10	4	8	5	4	200000	100	5	10	9	2			±15	Vol. A
TLE2301	40	9	2.2	3.5	15	10	260000	97	44	8	14	1			±15	Vol. B
TLV2361	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	1			±2.5	Vol. B
TLV2362	5	2	1.75	2.5	7.5	6	20000	85	8	7	3	2			±2.5	Vol. B
TLE2161	36	7	0.29	0.35	3.9	3	4	90	40	6.4	10	1			±15	Vol. B
TLE2161A	36	7	0.29	0.35	2.5	1.5	4	90	40	6.4	10	1			±15	Vol. B
TLE2161B	36	7	0.29	0.35	1	0.5	4	90	40	6.4	10	1			±15	Vol. B
TLE2141	44	4	3.5	4.5	1.3	0.9	–7000	108	10.5	5.9	45	1			±15	Vol. B
TLE2141A	44	4	3.5	4.5	0.8	0.5	–7000	108	10.5	5.9	45	1			±15	Vol. B
TLE2142	44	4	3.45	4.5	1.6	1.2	–7000	108	10.5	5.9	45	2			±15	Vol. B
TLE2142A	44	4	3.45	4.5	1.2	0.75	–7000	108	10.5	5.9	45	2			±15	Vol. B
TLE2144	44	4	3.45	4.5	3.2	2.4	–7000	108	10.5	5.9	45	4			±15	Vol. B
TLE2144A	44	4	3.45	4.5	2.4	1.5	–7000	108	10.5	5.9	45	4			±15	Vol. B
TLV2460	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2460A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1	Y	RRIO	3	2–127
TLV2461	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	1		RRIO	3	2–127

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)		V_{IO} (Max) (mV)		I_{IB} (Typ) (pA)	CMRR (Typ) (dB)	V_n @ 1 kHz (Typ) (nV/√Hz)	GBW (Typ) (MHz)	Slew Rate (Typ) (V/μs)	AMPS	SHDN	Rail to Rail	Spec'd at V_{CC} (V)	Ref.
	Max	Min	Typ	Max	Full Range	25°C										
TLV2461A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	1		RRIO	3	2–127
TLV2462	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2462A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2		RRIO	3	2–127
TLV2463	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2463A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	2	Y	RRIO	3	2–127
TLV2464	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2464A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4		RRIO	3	2–127
TLV2465	6	2.7	0.5	0.575	2.2	2	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2465A	6	2.7	0.5	0.575	1.7	1.5	4400	80	11	5.2	1.6	4	Y	RRIO	3	2–127
TLV2770	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2770A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1	Y	RRO	2.7	2–255
TLV2771	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	1		RRO	2.7	2–255
TLV2771A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	1		RRO	2.7	2–255
TLV2772	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2772A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2		RRO	2.7	2–255
TLV2773	5.5	2.5	1	2	2.7	2.5	2	84	21	4.8	9	2	Y	RRO	2.7	2–255
TLV2773A	5.5	2.5	1	2	1.9	1.6	2	84	21	4.8	9	2	Y	RRO	2.7	2–255
TLV2774	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4		RRO	2.7	2–255
TLV2774A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4		RRO	2.7	2–255
TLV2775	5.5	2.5	1	2	2.9	2.7	2	84	21	4.8	9	4	Y	RRO	2.7	2–255
TLV2775A	5.5	2.5	1	2	2.2	2.1	2	84	21	4.8	9	4	Y	RRO	2.7	2–255

Devices in **bold** are is this data book
Vol A – Amplifiers, Comparators, and Special Functions Data Book Volume A (SLYD011A); Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

PACKAGE AVAILABILITY

This package availability guide shows with an *X* the amplifiers that are available in the indicated package by product suffix code (e.g., TLV2461IDBV is a TLV2462 in the industrial temperature grade in a SOT-23 package). The following product suffix codes indicate the associated package.

Product Suffix Code	Package Type	Product Suffix Code	Package Type
D	SOIC (8, 14, or 16 pin)	J	CDIP (14 or 16 pin)
DBV	SOT-23 (5 or 6 pin)	JG	CDIP (8 pin)
DGK	MSOP (8 pin)	N	PDIP (14, 16, or 18 pin)
DGN	MSOP in PowerPAD™ (8 pin)	P	PDIP (8 pin)
DGQ	MSOP in PowerPAD™ (8 pin)	PW	TSSOP (8, 14, 16, 20, 24, or 28 pin)
DGS	MSOP (10 pin)	PWP	TSSOP in PowerPAD™ (20 pin)
FK	LCCC (20 pin)	U	CPAK (10 pin)

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DEVICE	D	DBV	DGK	DGN	DGQ	DGS	FK	J	JG	N	P	PW	PWP	U	Pg. No.
TL343		X													2–7
TL3472	X										X				2–13
TLC070	X			X							X				2–17
TLC070A	X										X				2–17
TLC071	X			X							X				2–17
TLC071A	X										X				2–17
TLC072	X			X							X				2–17
TLC072A	X				X						X				2–17
TLC073	X									X					2–17
TLC073A	X									X					2–17
TLC074	X									X		X	X		2–17
TLC074A	X									X		X	X		2–17
TLC075	X									X		X	X		2–17
TLC075A	X									X		X	X		2–17
TLC080	X			X							X				2–43
TLC080A	X										X				2–43
TLC081	X			X							X				2–43
TLC081A	X										X				2–43
TLC082	X			X							X				2–43
TLC082A	X										X				2–43

TEXAS INSTRUMENTS

DEVICE	D	DBV	DGK	DGN	DGQ	DGS	FK	J	JG	N	P	PW	PWP	U	Pg. No.
TLC083	X				X					X					2–43
TLC083A	X									X					2–43
TLC084	X									X			X		2–43
TLC084A	X									X			X		2–43
TLC085	X									X		X	X		2–43
TLC085A	X									X		X	X		2–43
TLV2422	X						X		X			X		X	2–69
TLV2422A	X						X		X			X		X	2–69
TLV2450	X	X									X				2–99
TLV2450A	X										X				2–99
TLV2451	X	X									X				2–99
TLV2451A	X										X				2–99
TLV2452	X		X								X				2–99
TLV2452A	X										X				2–99
TLV2453	X					X					X				2–99
TLV2453A	X										X				2–99
TLV2454	X										X		X		2–99
TLV2454A	X										X		X		2–99
TLV2455	X										X		X		2–99
TLV2455A	X										X		X		2–99
TLV2460	X	X									X				2–127
TLV2460A	X										X				2–127
TLV2461	X	X									X				2–127
TLV2461A	X										X				2–127
TLV2462	X		X								X				2–127
TLV2462A	X										X				2–127
TLV2463	X					X					X				2–127
TLV2463A	X										X				2–127
TLV2464	X										X		X		2–127
TLV2464A	X										X		X		2–127
TLV2465	X										X		X		2–127
TLV2465A	X										X		X		2–127
TLV2470	X	X									X				2–153

PACKAGE AVAILABILITY (continued)

DEVICE	D	DBV	DGK	DGN	DGQ	DGS	FK	J	JG	N	P	PW	PWP	U	Pg. No.
TLV2470A	X										X				2–153
TLV2471	X	X									X				2–153
TLV2471A	X										X				2–153
TLV2472	X			X							X				2–153
TLV2472A	X										X				2–153
TLV2473	X				X					X					2–153
TLV2473A	X									X					2–153
TLV2474	X									X				X	2–153
TLV2474A	X									X				X	2–153
TLV2475	X									X		X	X		2–153
TLV2475A	X									X		X	X		2–153
TLV2711		X													2–177
TLV2721		X													2–203
TLV2731		X													2–229
TLV2770	X		X								X				2–255
TLV2770A	X										X				2–255
TLV2771	X	X													2–255
TLV2771A	X														2–255
TLV2772	X		X				X		X		X			X	2–255
TLV2772A	X						X		X		X			X	2–255
TLV2773	X					X				X					2–255
TLV2773A	X									X					2–255
TLV2774	X										X	X			2–255
TLV2774A	X										X	X			2–255
TLV2775	X									X		X			2–255
TLV2775A	X									X		X			2–255

MSOP Package Codes Guide

Purpose: MSOP packages are too small to denote the full part number symbolization on the MSOP package. Following is a table of codes that appear on the MSOP packages for operational amplifiers. The *xx* preceding the 5-digit code designates a changing manufacturing code not needed for product identification, and will vary.

Example: An MSOP package that is physically stamped with *97TIABX* denotes that this is part number TLV2473IDGQ. These parts are also available on reels. Therefore this MSOP, reeled, would be orderable as TLV2473IDGQR.

Symbol	Orderable Part Number
xxTIACS	TLC070CDGN
xxTIACT	TLC070IDGN
xxTIACU	TLC071CDGN
xxTIACV	TLC071IDGN
xxTIADV	TLC072CDGN
xxTIADW	TLC072IDGN
xxTIADX	TLC073CDGQ
xxTIADY	TLC073IDGQ
xxTIACW	TLC080CDGN
xxTIACX	TLC080IDGN
xxTIACY	TLC081CDGN
xxTIACZ	TLC081IDGN
xxTIADZ	TLC082CDGN
xxTIAEA	TLC082IDGN
xxTIAEB	TLC083CDGN
xxTIAEC	TLC083IDGN
xxTIABI	TLV2452CDGK
xxTIABJ	TLV2452IDGK
xxTIABK	TLV2453CDGS
xxTIABL	TLV2453IDGS

Symbol	Orderable Part Number
xxTIAAI	TLV2462CDGK
xxTIAAJ	TLV2462IDGK
xxTIAAK	TLV2463CDGS
xxTIAAL	TLV2463IDGS
xxTIABU	TLV2472CDGN
xxTIABV	TLV2472IDGN
xxTIABW	TLV2473CDGQ
xxTIABX	TLV2473IDGQ
xxTIABO	TLV2770CDGK
xxTIABP	TLV2770IDGK
xxTIAAH	TLV2772AIDGK
xxTIAAF	TLV2772CDGK
xxTIAAG	TLV2772IDGK
xxTIABQ	TLV2773CDGS
xxTIABR	TLV2773IDGS
xxTIADL	TLV2782CDGK
xxTIADM	TLV2782IDGK
xxTIADN	TLV2783CDGS
xxTIADO	TLV2783IDGS
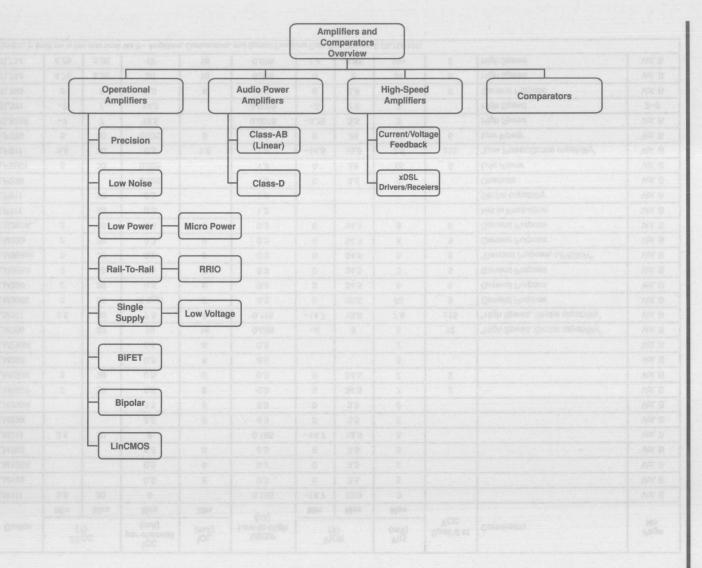
SOT-23 Package Codes Guide

Purpose: SOT-23 packages are too small to denote the full part number symbolization on the package. Following is a table of codes that appear on the SOT-23 packages for operational amplifiers.

Example: A SOT-23 package that is physically stamped with *VAOI* denotes that this is part number TLV2460CDBV. These parts are also available on reels. Therefore this SOT part is also orderable as TLV2460CDBVR.

Symbol	Orderable Part Number
TAAC	TL343CDBV
TAAI	TL343IDBV
VAAC	TLV2361CDBV
VAAI	TLV2361IDBV
VABC	TLV1391CDBV
VABI	TLV1391IDBV
VACC	TLV2211CDBV
VACI	TLV2211IDBV
VADC	TLV2221CDBV
VADI	TLV2221IDBV
VAEC	TLV2231CDBV
VAEI	TLV2231IDBV
VAFC	TLV2311CDBV
VAFI	TLV2311IDBV
VAGC	TLV2321CDBV
VAGI	TLV2321IDBV
VAJC	TLV2711CDBV
VAJI	TLV2711IDBV
VAKC	TLV2721CDBV

Symbol	Orderable Part Number
VAKI	TLV2721IDBV
VALC	TLV2731CDBV
VALI	TLV2731IDBV
VAMC	TLV2771CDBV
VAMI	TLV2771IDBV
VANI	TLV2771AIDBV
VAOC	TLV2460CDBV
VAOI	TLV2460IDBV
VAPC	TLV2461CDBV
VAPI	TLV2461IDBV
VAQC	TLV2450CDBV
VAQI	TLV2450IDBV
VARC	TLV2451CDBV
VARI	TLV2451IDBV
VAUC	TLV2470CDBV
VAUI	TLV2470IDBV
VAVC	TLV2471CDBV
VAVI	TLV2471IDBV

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

Amplifiers and Comparators Overview

- **Operational Amplifiers**
  - Precision
  - Low Noise
  - Low Power — Micro Power
  - Rail-To-Rail — RRIO
  - Single Supply — Low Voltage
  - BiFET
  - Bipolar
  - LinCMOS
- **Audio Power Amplifiers**
  - Class-AB (Linear)
  - Class-D
- **High-Speed Amplifiers**
  - Current/Voltage Feedback
  - xDSL Drivers/Receiers
- **Comparators**

1-53

COMPARATORS

Device	ΔV_{CC} (V)		I_{CC} per channel (mA)	I_{OL} (mA)	t_{RESP} Low-to-High (μs)	V_{ICR} (V)		V_{IO} (mV)	Spec'd at V_{CC}	Comments	Page No.
	Min	Max	Max	Min		Min	Max	Max			
LM111	3.5	30	6		0.165	−14.7	13.8	3			Vol. B
LM139			0.5	6	0.3	0	3.5	5			Vol. B
LM139A			0.5	6	0.3	0	3.5	2			Vol. B
LM193			0.5	6	0.3	0	3.5	5			Vol. B
LM211	3.5	30	6		0.165	−14.7	13.8	3			Vol. B
LM239			0.5	6	0.3	0	3.5	5			Vol. B
LM239A			0.5	6	0.3	0	3.5	2			Vol. B
LM2901	2	36	0.5	6	0.3	0	34.5	7	5		Vol. B
LM2903	2	36	0.5	6	0.3	0	34.5	7	5		Vol. B
LM293			0.5	6	0.3			5			Vol. B
LM293A			0.5	6	0.3			2			Vol. B
LM306		30	10	16	0.028	−5	5	5	12	"High Speed, Strobe capability"	Vol. B
LM311	3.5	30	7.5	8	0.115	−14.7	13.8	7.5	±15	"High Speed, Strobe capability"	Vol. B
LM3302	2	28	.2 (typ)	6	0.3	0	26.5	20	5	General Purpose	Vol. B
LM339	2	36	0.5	6	0.3	0	34.5	5	5	General Purpose	Vol. B
LM339A	2	36	0.5	6	0.3	0	34.5	3	5	General Purpose	Vol. B
LM339x2	2	36	0.5	6	0.3	0	34.5	5	5	"General Purpose, LIFEBUY"	Vol. B
LM393	2	36	0.5	6	0.3	0	34.5	5	5	General Purpose	Vol. B
LM393A	2	36	0.5	6	0.3	0	34.5	3	5	General Purpose	Vol. B
LP111		30	0.3		1.2					Not in Production	Vol. B
LP211		30	0.3		1.2					Strobe capability	Vol. B
LP239			0.025		1.3	0	3.5	5		Obsolete	Vol. B
LP2901	5	30	0.025		1.3	0	28	±5	5	Low Power	Vol. B
LP311	3.5	30	0.3	1.6	1.2	−14.5	13.5	7.5	±15	"Low Power, Strobe capability"	Vol. B
LP339	5	30	0.025	6	1.3	0	28	±5	5	Low Power	Vol. B
TL3016	−7	7	12.5		0.0078	−3.75	3.5	3		High Speed	Vol. B
TL331	−7	7	14.7		0.0099	−5	2.5	3		High Speed	2–3
TL393	2	7	0.5	6	0.2	0	5.8	5	5	General Purpose	Vol. B
TL712	4.75	5.25	20	16	0.025	0	5	5+	5	High Speed	Vol. B
TL714	4.75	5.25	12	16	0.006	1.4	3.85	10+	5	High Speed	Vol. B

Devices in **bold** are is this data book Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

TEXAS
INSTRUMENTS
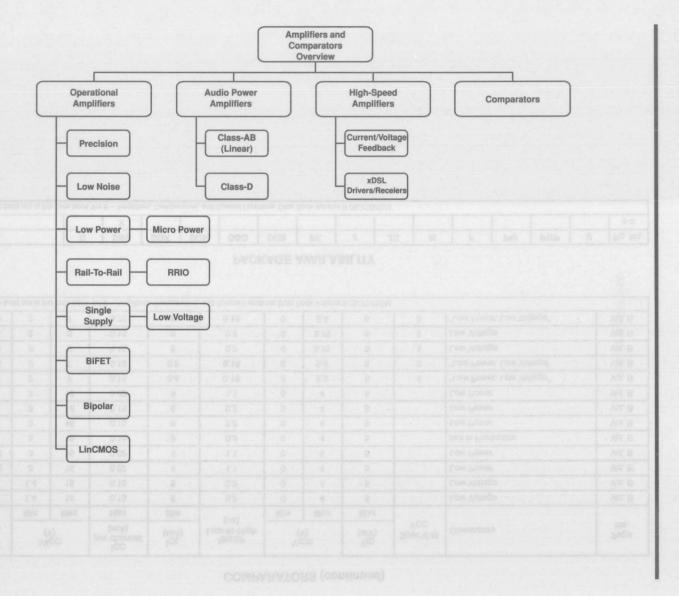
COMPARATORS (continued)

Device	ΔVCC (V) Min	ΔVCC (V) Max	ICC per channel (mA) Max	IOL (mA) Min	tRESP Low-to-High (µs)	VICR (V) Min	VICR (V) Max	VIO (mV) Max	Spec'd at VCC	Comments	Page No.
TLC352	1.4	16	0.15	6	0.2	0	4	5		Low Voltage	Vol. B
TLC354	1.4	16	0.15	6	0.2	0	4	5		Low Voltage	Vol. B
TLC3702	3	16	0.02	4	1.1	0	4	5		Low Power	Vol. B
TLC3704	3	16	0.02	4	1.1	0	4	5		Low Power	Vol. B
TLC371	3	16	0.15	6	0.2	0	4	5		Not in Production	Vol. B
TLC372	3	16	0.15	6	0.2	0	4	5		Low Power	Vol. B
TLC374	3	16	0.15	6	0.2	0	4	5		Low Power	Vol. B
TLC393	3	16	0.02	6	1.1	0	4	5		Low Power	Vol. B
TLV1391	2	7	0.15	0.6	0.18	0	5.8	5	5	"Low Power, Low Voltage"	Vol. B
TLV1393	2	7	0.15	0.6	0.18	0	5.8	5	5	"Low Power, Low Voltage"	Vol. B
TLV2352	2	8	0.15	6	0.2	0	3.75	5	5	Low Voltage	Vol. B
TLV2354	2	8	0.15	6	0.2	0	3.75	5	5	Low Voltage	Vol. B
TLV2393	2	7	0.75	6	0.15	0	5.8	5	5	"Low Power, Low Voltage"	Vol. B

Devices in **bold** are is this data book Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

PACKAGE AVAILABILITY

DEVICE	D	DBV	DGK	DGN	DGQ	DGS	FK	J	JG	N	P	PW	PWP	U	Pg. No.
TL331		X													2–3

Devices in **bold** are is this data book Vol B – Amplifiers, Comparators, and Special Functions Data Book Volume B (SLYD012A)

TEXAS
INSTRUMENTS

REPLACE COMPARATOR
SELECTION GUIDE

Amplifiers and Comparators Overview

- **Operational Amplifiers**
  - Precision
  - Low Noise
  - Low Power — Micro Power
  - Rail-To-Rail — RRIO
  - Single Supply — Low Voltage
  - BiFET
  - Bipolar
  - LinCMOS

- **Audio Power Amplifiers**
  - Class-AB (Linear)
  - Class-D

- **High-Speed Amplifiers**
  - Current/Voltage Feedback
  - xDSL Drivers/Receivers

- **Comparators**

Class AB Audio Power Amplifiers†

Part No	Output Power (W)	THD + N @ 1 kHz	V_{CC}/V_{DD} (min) (V)	V_{CC}/V_{DD} (max) (V)	I_{DD}/I_{CC} per channel (typ) (mA)	PSRR (dB)	Shutdown Control (typ) (uA)	ISD (uA)	Description
TPA0102	1.5	0.05	3	5.5	10	75	5	5	BTL, SE, Stereo
TPA0103	1.75	0.05	3	5.5	10	75	5	5	BTL, SE, Stereo
TPA0112	2	0.75	4.5	5.5	3	77	100	150	BTL, Depop, SE, Stereo
TPA0122	2	0.1	4.5	5.5	9	77	100	100	BTL, Depop, SE, Stereo
TPA0132	2	0.4	4.5	5.5	5	67	100	150	BTL, Depop, SE, Stereo
TPA0142	2	0.05	4.5	5.5	10	67	100	100	BTL, Depop, SE, Stereo
TPA0152	2	0.05	4.5	5.5	5	67	100	100	BTL, Depop, SE, Stereo
TPA0162	2	0.05	4.5	5.5	10	67	100	100	BTL, Depop, SE, Stereo
TPA0202	2	0.05	3	5.5	10	75	5	5	BTL, Depop, SE, Stereo
TPA102	0.15	0.05	2.5	5.5	0.75	76	60	60	Depop, SE, Stereo
TPA112	0.15	0.05	2.5	5.5	0.75	76			SE, Stereo
TPA122	0.15	0.05	2.5	5.5	0.75	76	60	60	Depop, SE, Stereo
TPA152	0.075	0.02	4.5	5.5	3	81			Depop, SE, Stereo
TPA301	0.35	0.3	2.5	5.5	0.7	78	0.15	0.15	BTL, Mono
TPA302	0.3	0.08	2.7	5.5	2	65	0.6	0.6	SE, Stereo
TPA311	0.35	0.3	2.5	5.5	0.7	78	7	7	BTL, Depop, Mono, SE
TPA701	0.7	0.2	2.5	5.5	1.25	85	0.0015	0.0015	BTL, Mono
TPA711	0.7	0.2	2.5	5.5	1.25	85	50	50	BTL, Mono, SE
TPA721	0.7	0.2	2.5	5.5	1.25	85	50	50	BTL, Depop, Mono
TPA1517	6	10	9.5	18	20	65	7	7	SE, Stereo
TPA4860	1	0.3	2.7	5.5	3.5	75	0.6	0.6	BTL, Mono
TPA4861	1	0.3	2.7	5.5	3.5	75	0.6	0.6	BTL, Mono

† Data sheets for these devices can be found in the Audio Power Amplifiers Data Book (Literature Number SLOD004).

Class-D Audio Power Amplifiers[†]

Part No	Output Power (W)	THD + N @ 1 kHz	V_{CC}/V_{DD} (min) (V)	V_{CC}/V_{DD} (max) (V)	I_{DD}/I_{CC} per channel (typ) (mA)	PSRR (dB)	Shutdown Control (typ) (uA)	ISD (uA)	Description
TPA005D02	2	0.4	4.5	5.5	12	40	400	400	Class–D, Stereo
TPA005D12	2	0.5	4.5	5.5	12.5	40	0.2	0.2	Class–D, Stereo
TPA005D14	2	0.5	4.5	5.5	12.5	40	0.2	0.2	Class–D, Stereo

[†] Data sheets for these devices can be found in the Audio Power Amplifiers Data Book (Literature Number SLOD004).

Current/Voltage Feedback High-Speed Amplifiers†

Part No	V_{CC}/V_{DD} 5 (V)	V_{CC}/V_{DD} ±5 (V)	V_{CC}/V_{DD} ±15 (V)	ACL, min Stable Gain (V/V)	BW at ACL (MHz)	Slew Rate (V/µs)	Settling Time (0.1%) (typ) (ns)	THD FC=1 MHz (typ) (dB)	V_n (typ) (nV/√Hz)	Diff Gain (%)	Diff Phase (deg)	Description
THS3001	No	Yes	Yes	1	420	6500	40	−96		0.01	0.02	Current Feedback
THS3002	No	Yes	Yes	1	420	6500	40	−96		0.01	0.02	Current Feedback
THS4001	Yes	Yes	Yes	1	270	400	40	−72	12.5	0.04	0.15	Voltage Feedback
THS4011				1	290	310	37		7.5	0.006	0.01	PowerPAD Package, Sub–miniature Package, Voltage Feedback
THS4012				1	290	310	37		7.5	0.006	0.01	PowerPAD Package, Sub–miniature Package, Voltage Feedback
THS4031				1	100	100	60		1.6	0.015	0.025	PowerPAD Package, Sub–miniature Package, Voltage Feedback
THS4032	No			2	100	100	60		1.6	0.015	0.025	PowerPAD Package, Sub–miniature Package, Voltage Feedback
THS4051				1	70	240	60		14	0.01	0.01	PowerPAD Package, Sub–miniature Package, Voltage Feedback
THS4052				1	70	240	60		14	0.01	0.01	PowerPAD Package, Sub–miniature Package, Voltage Feedback
THS4061				1	180	400	40		14.5	0.02	0.02	PowerPAD Package, Sub–miniature Package, Voltage Feedback
THS4062				1	180	400	40		14.5	0.02	0.02	PowerPAD Package, Sub–miniature Package, Voltage Feedback
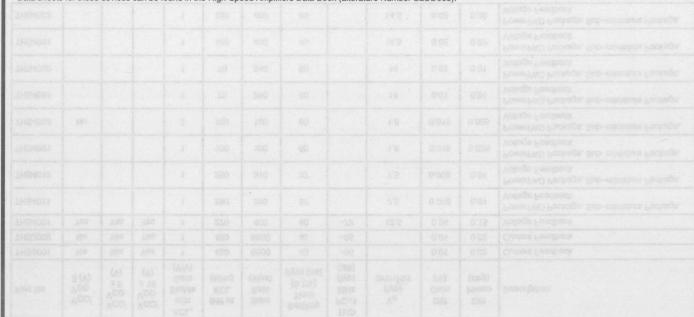
† Data sheets for these devices can be found in the High-Speed Amplifiers Data Book (Literature Number SLOD005).

xDSL High-Speed Drivers/Receivers†

Part No	V_{CC}/V_{DD} ±5 (V)	V_{CC}/V_{DD} ±15 (V)	BW at ACL (MHz)	Slew Rate (V/μs)	V_n (typ) (nV/√Hz)	THD FC=1 MHz (typ) (dB)	I_O (typ) (mA)	Description
THS6002	Yes	Yes	140	1000		−62	480	PowerPAD Package, xDSL Amplifiers
THS6012	Yes	Yes	140	1300		−65	500	PowerPAD Package, xDSL Amplifiers
THS6022	Yes	Yes	210	1900		−65	250	PowerPAD Package, Sub–miniature Package, xDSL Amplifiers
THS6062	Yes	Yes	100	100	1.6	−84	90	PowerPAD Package, Sub–miniature Package, Voltage Feedback, xDSL Amplifiers
THS7001			75	175	1.7	−84	50	PGA, PowerPAD Package, SHUTDOWN, Sub–miniature Package, Voltage Feedback, xDSL Amplifiers
THS7002			75	175	1.7	−84	50	PGA, PowerPAD Package, SHUTDOWN, Sub–miniature Package, Voltage Feedback, xDSL Amplifiers

† Data sheets for these devices can be found in the High-Speed Amplifiers Data Book (Literature Number SLOD005).

α_{IIO} Average Temperature Coefficient of Input Offset Current

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range.

$$\alpha_{IIO} = \frac{\left(I_{IO} \text{ at } T_{A(1)}\right) - \left(I_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

α_{VIO} Average Temperature Coefficient of Input Offset Voltage

The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range. The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

$$\alpha_{VIO} = \frac{\left(V_{IO} \text{ at } T_{A(1)}\right) - \left(V_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$

where $T_{A(1)}$ and $T_{A(2)}$ are the specified temperature extremes.

ΔV_{CC}

See k_{SVS}

ΔV_{IO}

See k_{SVS}

ϕ_m Phase Margin

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.

A_m Gain Margin

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.

A_V Large-Signal Voltage Amplification

The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output

A_{VD} Differential Voltage Amplification

The ratio of the change in output to the change in differential input voltage producing it with the common-mode input voltage held constant

B_1 Unity-Gain Bandwidth

The range of frequencies within which the maximum output voltage swing is above a specified value.

B_{OM} Maximum-Output-Swing Bandwidth

The range of frequencies within which the maximum output voltage swing is above the specified value.

c_i Input Capacitance

The capacitance between the input terminals with either input grounded

OPERATIONAL AMPLIFIER
GLOSSARY

CMRR, k_{CMR}
Common-Mode Rejection Ratio

The ratio of differential voltage amplification to common-mode voltage amplification.

NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

$\overline{F}$ **Average Noise Figure**

The ratio of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

I_{CC+}, I_{CC-}
Supply Current

The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit

I_{IB}   **Input Bias Current**

The average of the currents into the two input terminals with the output at the specified level

I_{IO}   **Input Offset Current**

The difference between the currents into the two input terminals with the output at the specified level

I_n   **Equivalent Input Noise Current**

The current of an ideal current source (having internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.

I_{OL}   **Low-Level Output Current**

The current into an output with input conditions applied that according to the product specification will establish a low level at the output.

I_{OS}   **Short-Circuit Output Current**

The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point

k_{CMR}

See CMRR

k_{SVS}, ΔV_{CC}, ΔV_{IO}
Supply Voltage Sensitivity

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.

NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

k_{SVR}   **Supply Voltage Rejection Ratio**

The absolute value of the ratio of the change in supply voltages to the change in input offset voltage.

NOTES: 1. Unless otherwise noted, both supply voltages are varied symmetrically.
2. This is the reciprocal of supply voltage sensitivity.

P_D   **Total Power Dissipation**

The total dc power supplied to the device less any power delivered from the device to a load.

NOTE: At no load: $P_D = V_{CC+} \bullet I_{CC+} + V_{CC-} \bullet I_{CC-}$

r_i   **Input Resistance**

The resistance between the input terminals and either input grounded

r_{id}   **Differential Input Resistance**

The small-signal resistance between two ungrounded input terminals

r_o   **Output Resistance**

The resistance between an output terminal and ground

SR   **Slew Rate**

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input

t_r   **Rise Time**

The time required for an output voltage step to change from 10% to 90% of its final value

t_{tot}   **Total Response Time**

The time between a step-function change of the input signal and the instant at which the magnitude of the output signal reaches for the last time a specified level range (±ε) containing the final output signal level.

V_I   **Input Voltage Range**

The range of voltage that if exceeded at either input terminal may cause the operational amplifier to cease functioning properly.

V_{IO}   **Input Offset Voltage**

The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.

V_{IC}   **Common-Mode Input Voltage**

The average of the two input voltages

V_{ICR}   **Common-Mode Input Voltage Range**

The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.

V_n   **Equivalent Input Noise Voltage**

The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.

V_{O1}/V_{O2}   **Crosstalk Attenuation**

The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel

V_{OH}   **High-Level Output Voltage**

The voltage at an output with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL}   **Low-Level Output Voltage**

The voltage at an output with input conditions applied that according to the product specification will establish a low level at the output.

OPERATIONAL AMPLIFIER
GLOSSARY

V$_{ID}$ **Differential Input Voltage**

The voltage at the noninverting input with respect to the inverting input

V$_{OM}$ **Maximum Peak Output Voltage Swing**

The maximum positive or negative peak output voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

V$_{O(PP)}$ **Maximum Peak-to-Peak Output Voltage Swing**

The maximum peak-to-peak output voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.

z$_{ic}$ **Common-Mode Input Impedance**

The parallel sum of the small-signal impedance between each input terminal and ground

z$_o$ **Output Impedance**

The small-signal impedance between the output terminal and ground

Overshoot Factor

The ratio of the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal to the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

Contents

2

Data Sheets

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage
  . . . 2 V to 36 V
- Low Supply-Current Drain Independent of Supply Voltage . . . 0.5 mA Typ
- Low Input Bias Current . . . 25 nA Typ
- Low Input Offset Voltage . . . 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage . . . ±36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS
- Packaged in Plastic Small-Outline Transistor Package

DBV PACKAGE
(TOP VIEW)

```
         ┌───────┐
IN(−) ──┤ 1    5 ├── V_CC
        │        │
V_CC/GND┤ 2      │
        │        │
IN(+) ──┤ 3    4 ├── OUT
         └───────┘
```

description

This device consists of a single voltage comparator that is designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible if the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The output can be connected to other open-collector outputs to achieve wired-AND relationships.

The TL331I is characterized for operation from −40°C to 85°C.

logic diagram

```
IN+ ──────│‾‾‾\
          │    >o──── OUT
IN− ──────│___/
```

AVAILABLE OPTIONS
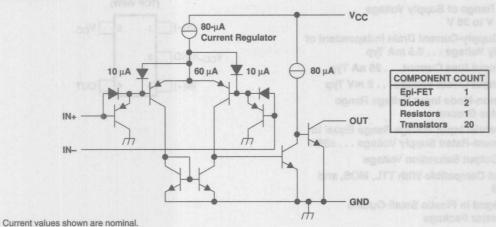
T_A	$V_{IO}(max)$ AT 25°C	PACKAGED DEVICE SMALL-OUTLINE TRANSISTOR (DBV)
−40°C to 85°C	5 mV	TL331IDBV

The DBV package is only available left-end taped and reeled. Add R suffix to device type (e.g., TL331IDBVR).

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TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

schematic

COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Current values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1) .... 36 V
Differential input voltage, V_{ID} (see Note 2) .... ±36 V
Input voltage range, V_I (either input) .... –0.3 V to 36 V
Output voltage, V_O .... 36 V
Output current, I_O .... 20 mA
Duration of output short-circuit to ground (see Note 3) .... unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5) .... 347°C/W
Operating free-air temperature range, T_A .... –40°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V, V_{IC} = $V_{IC(min)}$		25°C		2	5	mV
				−40°C to 85°C			9	
I_{IO}	Input offset current	V_O = 1.4 V		25°C		5	50	nA
				−40°C to 85°C			250	
I_{IB}	Input bias current	V_O = 1.4 V		25°C		−25	−250	nA
				−40°C to 85°C			−400	
V_{ICR}	Common-mode input voltage range‡			25°C		0 to V_{CC}−1.5		V
				−40°C to 85°C		0 to V_{CC}−2		
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, R_L ≥ 15 kΩ to V_{CC}		25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V,	V_{ID} = 1 V	25°C		0.1	50	nA
		V_{OH} = 30 V,	V_{ID} = 1 V	−40°C to 85°C			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA,	V_{ID} = −1 V	25°C		150	400	mV
				−40°C to 85°C			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V,	V_{ID} = 1 V	25°C	6			mA
I_{CC}	Supply current	R_L = ∞,	V_{CC} = 5 V	25°C		0.4	0.7	mA

† All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

‡ The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} − 1.5 V, but either or both inputs can go to 30 V without damage.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF§, See Note 6	100-mV input step with 5-mV overdrive		1.3		µs
		TTL-level input step		0.3		

§ C_L includes probe and jig capacitance.

NOTE 6: The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

- **Wide Range of Supply Voltages, Single Supply . . . 3 V to 36 V, or Dual Supplies**
- **Class AB Output Stage**
- **True Differential-Input Stage**
- **Low Input Bias Current**
- **Internal Frequency Compensation**
- **Short-Circuit Protection**
- **Packaged in SOT-23 Package**

DBV PACKAGE
(TOP VIEW)

```
IN+    [ 1      5 ]  VCC+
VCC/GND [ 2
IN−    [ 3      4 ]  OUT
```

description

The TL343 is a single operational amplifier similar in performance to the µA741, but with several distinct advantages. It is designed to operate from a single supply over a range of voltages from 3 V to 36 V. Operation from split supplies also is possible, provided the difference between the two supplies is 3 V to 36 V. The common-mode input range includes the negative supply. Output range is from the negative supply to $V_{CC} - 1.5$ V.

The TL343 is characterized for operation from −40°C to 125°C.

symbol

```
IN+  ———————| +
                |———  OUT
IN−  ———————| −
```

AVAILABLE OPTIONS
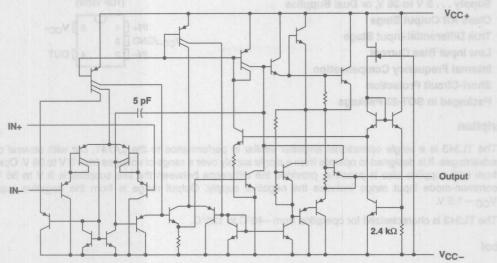
TA	V$_{IO}$MAX AT 25°C	PACKAGE SOT–23 (DBV)
−40°C to 125°C	10 mV	TL343IDBV

The DBV package is only available taped and reeled. Add R suffix to device type for ordering (e.g., TL343IDBVR).

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TEXAS INSTRUMENTS

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TL343
SINGLE LOW-POWER OPERATIONAL AMPLIFIER

schematic

NOTE A. Component values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		MAX	UNIT
Supply voltage (see Note 1)	V_{CC+}	18	V
	V_{CC-}	−18	
Supply voltage, V_{CC+} with respect to V_{CC-}		36	V
Differential input voltage (see Note 2)		±36	V
Input voltage (see Notes 1 and 3)		±18	V
Package thermal impedance, θ_{JA} (see Note 4)	DBV package	347	°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
Storage temperature range		−65 to 150	°C

NOTES: 1. These voltage values are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN−.
3. Neither input must ever be more positive than V_{CC+} or more negative than V_{CC-}.
4. The package thermal impedance is calculated in accordance with JESD 51.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

recommended operating conditions

			MIN	MAX	UNIT
Single-supply voltage		V_{CC}	5	30	V
Dual-supply voltage		V_{CC+}	2.5	15	V
		V_{CC-}	−2.5	−15	
Operating free-air temperature, T_A			−40	125	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	See Note 5	25°C		2	10	mV
			Full range			12	
α_{VIO}	Temperature coefficient of input offset voltage	See Note 5	Full range		10		µV/°C
I_{IO}	Input offset current	See Note 5	25°C		30	50	nA
			Full range			200	
α_{IIO}	Temperature coefficient of input offset current	See Note 5	Full range		50		pA/C
I_{IB}	Input bias current	See Note 5	25°C		−0.2	−0.5	µA
			Full range			−0.8	
V_{ICR}	Common-mode input voltage range[‡]		25°C	V_{CC-} to 13	V_{CC-} to 13.5		V
V_{OM}	Peak output-voltage swing	$R_L = 10$ kΩ	25°C	±12	±13.5		V
		$R_L = 2$ kΩ	25°C	±10	±13		
		$R_L = 2$ kΩ	Full range	±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 2$ kΩ	25°C	20	200		V/mV
			Full range	15			
B_{OM}	Maximum-output-swing bandwidth	$V_{OPP} = 20$ V, $A_{VD} = 1$, THD $\leq 5\%$, $R_L = 2$ kΩ	25°C		9		kHz
B_1	Unity-gain bandwidth	$V_O = 50$ mV, $R_L = 10$ kΩ	25°C		1		MHz
ϕ_m	Phase margin	$C_L = 200$ pF, $R_L = 2$ kΩ	25°C		44°		
r_i	Input resistance	$f = 20$ Hz	25°C	0.3	1		MΩ
r_o	Output resistance	$f = 20$ Hz	25°C		75		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70	90		dB
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm2.5$ to ±15 V	25°C		30	150	µV/V
I_{OS}	Short-circuit output current[§]		25°C	±10	±30	±55	mA
I_{CC}	Total supply current	No load, See Note 5	25°C		0.7	2.8	mA

[†] All characteristics are measured under open-loop conditions with zero common-mode voltage unless otherwise specified. Full range for T_A is −40°C to 125°C.

[‡] The V_{ICR} limits are linked directly, volt-for-volt, to supply voltage; the positive limit is 2 V less than V_{CC+}.

[§] Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

NOTE 5: V_{IO}, I_{IO}, I_{IB}, and I_{CC} are defined at $V_O = 0$.

TL343
SINGLE LOW-POWER OPERATIONAL AMPLIFIER

electrical characteristics, V_{CC+} = 5 V, V_{CC-} = 0 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 2.5 V		2	10	mV
I_{IO}	Input offset current	V_O = 2.5 V		30	50	nA
I_{IB}	Input bias current	V_O = 2.5 V		−0.2	−0.5	µA
V_{OM}	Peak output voltage swing‡	R_L = 10 kΩ	3.3	3.5		V
A_{VD}	Large-signal differential voltage amplification	V_O = 1.7 V to 3.3 V, R_L = 2 kΩ	20	200		V/mV
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	$V_{CC\pm}$ = ± 2.5 V to ±15 V			150	µV/V
I_{CC}	Supply current	V_O = 2.5 V, No load		0.7	1.75	mA

† All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified.
‡ Output will swing essentially to ground.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C, A_{VD} = 1 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = ±10 V,	C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		1		V/µs
t_r	Rise time	See Note 5				0.35		µs
t_f	Fall time	ΔV_O = 50 mV,	C_L = 100 pF,	R_L = 10 kΩ, See Figure 1		0.35		µs
	Overshoot factor					20%		
	Crossover distortion	$V_{I(PP)}$ = 30 mV,	V_{OPP} = 2 V,	f = 10 kHz		1%		

PARAMETER MEASUREMENT INFORMATION
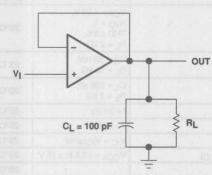
Figure 1. Unity-Gain Amplifier

TYPICAL CHARACTERISTICS†

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

Figure 2

INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE

Figure 3

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

Figure 4

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 5

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TL343
SINGLE LOW-POWER OPERATIONAL AMPLIFIER

SLOS250C – JUNE 1999 – REVISED JULY 1999

TYPICAL CHARACTERISTICS†

**LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY**

Figure 6

**VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE**

Figure 7

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

2–12

- Wide Gain-Bandwidth Product . . . 4 MHz
- High Slew Rate . . . 13 V/μs
- Fast Settling Time . . . 1.1 μs to 0.1%
- Wide-Range Single-Supply Operation . . . 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground (V$_{CC-}$)
- Low Total Harmonic Distortion . . . 0.035%
- Large-Capacitance Drive Capability . . . 10,000 pF
- Output Short-Circuit Protection

D OR P PACKAGE
(TOP VIEW)

1OUT	1	8	V$_{CC+}$
1IN–	2	7	2OUT
1IN+	3	6	2IN–
V$_{CC-}$/GND	4	5	2IN+

description

Quality, low-cost, bipolar fabrication with innovative design concepts are employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V$_{CC-}$). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

The TL3472C is characterized for operation from 0°C to 70°C. The TL3472I is characterized for operation from –40°C to 105°C.

AVAILABLE OPTIONS

	PACKAGED DEVICES	
T$_A$	SMALL OUTLINE (D)	PLASTIC DUAL-IN-LINE (P)
0°C to 70°C	TL3472CD	TL3472CP
–40°C to 105°C	TL3472ID	TL3472IP

D package is available taped and reeled. Add R suffix to device type for ordering (e.g., TL3472CDR).

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TL3472
HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200B – OCTOBER 1997 – REVISED JULY 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1)	18 V
$\qquad\qquad\quad V_{CC-}$	−18 V
Differential input voltage, V_{ID} (see Note 2)	±36 V
Input voltage, V_I (any input)	$V_{CC\pm}$
Input current, I_I (each input)	±1 mA
Output current, I_O	±80 mA
Total current into V_{CC+}	80 mA
Total current out of V_{CC-}	80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package	197°C/W
$\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad$ P package	104°C/W
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V_{CC-} − 0.3 V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{CC\pm}$		4	36	V
Common-mode input voltage, V_{IC}	V_{CC} = 5 V	0	2.8	V
	$V_{CC\pm}$ = ±15 V	−15	12.8	
Operating free-air temperature, T_A	TL3472C	0	70	°C
	TL3472I	−40	105	

TEXAS INSTRUMENTS

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electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage		$V_{CC} = 5$ V	25°C		1.5	10	mV
			$V_{CC} = \pm15$ V	25°C		1.0	10	
				Full range‡			12	
αV_{IO}	Temperature coefficient of input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50$ Ω	$V_{CC} = \pm15$ V	Full range‡		10		µV/°C
I_{IO}	Input offset current		$V_{CC} = \pm15$ V	25°C		6	75	nA
				Full range‡			300	
I_{IB}	Input bias current		$V_{CC} = \pm15$ V	25°C		100	500	µA
				Full range‡			700	
V_{ICR}	Common-mode input voltage range	$R_S = 50$ Ω		25°C		−15 to 12.8		V
				Full range‡		−15 to 12.8		
V_{OH}	High-level output voltage	$V_{CC+} = 5$ V, $V_{CC-} = 0$, $R_L = 2$ kΩ		25°C	3.7	4		V
		$R_L = 10$ kΩ		25°C	13.6	14		
		$R_L = 2$ kΩ		Full range‡	13.4			
V_{OL}	Low-level output voltage	$V_{CC+} = 5$ V, $V_{CC-} = 0$, $R_L = 2$ kΩ		25°C		0.1	0.3	V
		$R_L = 10$ kΩ		25°C		−14.7	−14.3	
		$R_L = 2$ kΩ		Full range‡			−13.5	
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 2$ kΩ		25°C	25	100		V/mV
				Full range‡	20			
I_{OS}	Short-circuit output current	Source: $V_{ID} = 1$ V, $V_O = 0$		25°C	−10	−34		mA
		Sink: $V_{ID} = -1$ V, $V_O = 0$			20	27		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$(min), $R_S = 50$ Ω		25°C	65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm13.5$ V to ±16.5 V, $R_S = 100$ Ω		25°C	70	97		dB
I_{CC}	Supply current (per channel)	$V_O = 0$, No load		25°C		3.5	4.5	mA
				Full range‡		4.5	5.5	
		$V_{CC+} = 5$ V, $V_O = 2.5$ V, $V_{CC-} = 0$, No load		25°C		3.5	4.5	

† All typical values are at $T_A = 25$°C.
‡ Full range is 0°C to 70°C for the TL3472C device and −40°C to 105°C for the TL3472I device.

TL3472
HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200B – OCTOBER 1997 – REVISED JULY 1999

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_I = -10$ V to 10 V, $R_L = 2$ kΩ, $C_L = 300$ pF	$A_V = 1$	8	10		V/μs
SR–	Negative slew rate		$A_V = -1$		13		
t_s	Settling time	$A_{VD} = -1$, 10-V step	To 0.1%		1.1		μs
			To 0.01%		2.2		
V_n	Equivalent input noise voltage	$f = 1$ kHz, $R_S = 100$ Ω			49		nV/√Hz
I_n	Equivalent input noise current	$f = 1$ kHz			0.22		pA/√Hz
THD	Total harmonic distortion	$V_O = 2$ V to 20 V, $R_L = 2$ kΩ, $A_{VD} = 10$, $f = 10$ kHz			0.02		%
GBW	Gain-bandwidth product	$f = 100$ kHz		3	4		MHz
BW	Power bandwidth	$V_{O(PP)} = 20$ V, $R_L = 2$ kΩ, $A_{VD} = 1$, THD = 5.0%			160		kHz
ϕ_m	Phase margin	$R_L = 2$ kΩ,	$C_L = 0$		70°		
		$R_L = 2$ kΩ,	$C_L = 300$ pF		50°		
	Gain margin	$R_L = 2$ kΩ,	$C_L = 0$		12		dB
		$R_L = 2$ kΩ,	$C_L = 300$ pF		4		
r_i	Differential input resistance	$V_{IC} = 0$			150		MΩ
C_i	Input capacitance	$V_{IC} = 0$			2.5		pF
	Channel separation	$f = 10$ kHz			101		dB
z_o	Open-loop output impedance	$f = 1$ MHz,	$A_V = 1$		20		Ω

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS

SLOS219B – JUNE 1999 – REVISED NOVEMBER 1999

- Wide Bandwidth . . . 10 MHz
- High Output Drive
  - I_{OH} . . . 57 mA at V_{DD} – 1.5
  - I_{OL} . . . 55 mA at 0.5 V
- High Slew Rate
  - SR+ . . . 16 V/μs
  - SR– . . . 19 V/μs
- Wide Supply Range . . . 4.5 V to 16 V
- Supply Current . . . 1.9 mA/Channel
- Ultra-Low Power Shutdown Mode
  I_{DD} . . . 125 μA/Channel
- Low Input Noise Voltage . . . 7 nV/$\sqrt{Hz}$
- Input Offset Voltage . . . 60 μV
- Ultra-Small Packages
  - 8 or 10 Pin MSOP (TLC070/1/2/3)

TLC070
D, DGN OR P PACKAGE
(TOP VIEW)

```
NULL  [ 1      8 ]  SHDN
IN–   [ 2      7 ]  V_DD
IN+   [ 3      6 ]  OUT
GND   [ 4      5 ]  NULL
```

description

Introducing the first members of TI's new BiMOS general-purpose operational amplifier family—the TLC07x. The BiMOS family concept is simple: provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher ac and dc performance. With performance rated from 4.5 V to 16 V across commercial (0°C to 70°C) and an extended industrial temperature range (–40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial and instrumentation applications. Familiar features like offset nulling pins, and new features like MSOP PowerPAD™ packages and shutdown modes, enable higher levels of performance in a multitude of applications.

Developed in TI's patented LBC3 BiCMOS process, the new BiMOS amplifiers combine a very high input impedance low-noise CMOS front end with a high-drive Bipolar output stage—thus providing the optimum performance features of both. AC performance improvements over the TL07x BiFET predecessors include a bandwidth of 10 MHz (an increase of 300%) and voltage noise of 7 nV/$\sqrt{Hz}$ (an improvement of 60%). DC improvements include a factor of 4 reduction in input offset voltage down to 1.5 mV (maximum) in the standard grade, and a power supply rejection improvement of greater than 40 dB to 130 dB. Added to this list of impressive features is the ability to drive ±50-mA loads comfortably from an ultra-small-footprint MSOP PowerPAD package, which positions the TLC07x as the ideal high-performance general-purpose operational amplifier family.

FAMILY PACKAGE TABLE

DEVICE	NO. OF CHANNELS	PACKAGE TYPES				SHUTDOWN	UNIVERSAL EVM BOARD
		MSOP	PDIP	SOIC	TSSOP		
TLC070	1	8	8	8	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLC071	1	8	8	8	—		
TLC072	2	8	8	8	—	—	
TLC073	2	10	14	14	—	Yes	
TLC074	4	—	14	14	20	—	
TLC075	4	—	16	16	20	Yes	

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TEXAS INSTRUMENTS

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TLC070 and TLC071 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	PACKAGED DEVICES		
	SMALL OUTLINE (D)†	SMALL OUTLINE (DGN)†	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	TLC070CD TLC071CD	TLC070CDGN TLC071CDGN	xxTIACS xxTIACU	TLC070CP TLC071CP
−40°C to 125°C	TLC070ID TLC071ID	TLC070IDGN TLC071IDGN	xxTIACT xxTIACV	TLC070IP TLC071IP
	TLC070AID TLC071AID	—	—	TLC070AIP TLC071AIP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC070CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLC072 and TLC073 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES						
	SMALL OUTLINE (D)†	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
		(DGN)†	SYMBOL§	(DGQ)†	SYMBOL§		
0°C to 70°C	TLC072CD TLC073CD	TLC072CDGN —	xxTIADV	— TLC073CDGQ	xxTIADX	— TLC073CN	TLC072CP —
−40°C to 125°C	TLC072ID TLC073ID	TLC072IDGN —	xxTIADW	— TLC073IDGQ	xxTIADY	— TLC073IN	TLC072IP —
	TLC072AID TLC073AID	—	—	—	—	— TLC073AIN	TLC072AIP —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC072CDR).
‡ Chip forms are tested at T_A = 25°C only.
§ xx represents the device date code.

TLC074 and TLC075 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PWP)†
0°C to 70°C	TLC074CD TLC075CD	TLC074CN TLC075CN	TLC074CPWP TLC075CPWP
−40°C to 125°C	TLC074ID TLC075ID	TLC074IN TLC075IN	TLC074IPWP TLC075IPWP
	TLC074AID TLC075AID	TLC074AIN TLC075AIN	TLC074AIPWP TLC075AIPWP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC074CDR).
‡ Chip forms are tested at T_A = 25°C only.

TEXAS INSTRUMENTS

TLC07x PACKAGE PINOUTS

TLC070
D, DGN OR P PACKAGE
(TOP VIEW)

NULL 1	8 $\overline{\text{SHDN}}$
IN– 2	7 V_{DD}
IN+ 3	6 OUT
GND 4	5 NULL

TLC071
D, DGN OR P PACKAGE
(TOP VIEW)

NULL 1	8 NC
IN– 2	7 V_{DD}
IN+ 3	6 OUT
GND 4	5 NULL

TLC072
D, DGN, OR P PACKAGE
(TOP VIEW)

1OUT 1	8 V_{DD}
1IN– 2	7 2OUT
1IN+ 3	6 2IN–
GND 4	5 2IN+

TLC073
DGQ PACKAGE
(TOP VIEW)

1OUT 1	10 V_{DD}
1IN– 2	9 2OUT
1IN+ 3	8 2IN–
GND 4	7 2IN+
$\overline{\text{1SHDN}}$ 5	6 $\overline{\text{2SHDN}}$

TLC073
D OR N PACKAGE
(TOP VIEW)

1OUT 1	14 V_{DD}
1IN– 2	13 2OUT
1IN+ 3	12 2IN–
GND 4	11 2IN+
NC 5	10 NC
$\overline{\text{1SHDN}}$ 6	9 $\overline{\text{2SHDN}}$
NC 7	8 NC

TLC074
D OR N PACKAGE
(TOP VIEW)

1OUT 1	14 4OUT
1IN– 2	13 4IN–
1IN+ 3	12 4IN+
V_{DD} 4	11 GND
2IN+ 5	10 3IN+
2IN– 6	9 3IN–
2OUT 7	8 3OUT

TLC074
PWP PACKAGE
(TOP VIEW)

1OUT 1	20 4OUT
1IN– 2	19 4IN–
1IN+ 3	18 4IN+
VDD 4	17 GND
2IN+ 5	16 3IN+
2IN– 6	15 3IN–
2OUT 7	14 3OUT
NC 8	13 NC
NC 9	12 NC
NC 10	11 NC

TLC075
D OR N PACKAGE
(TOP VIEW)

1OUT 1	16 4OUT
1IN– 2	15 4IN–
1IN+ 3	14 4IN+
V_{DD} 4	13 GND
2IN+ 5	12 3IN+
2IN– 6	11 3IN–
2OUT 7	10 3OUT
$\overline{\text{1/2SHDN}}$ 8	9 $\overline{\text{3/4SHDN}}$

TLC075
PWP PACKAGE
(TOP VIEW)

1OUT 1	20 4OUT
1IN– 2	19 4IN–
1IN+ 3	18 4IN+
VDD 4	17 GND
2IN+ 5	16 3IN+
2IN– 6	15 3IN–
2OUT 7	14 3OUT
$\overline{\text{1/2SHDN}}$ 8	13 $\overline{\text{3/4SHDN}}$
NC 9	12 NC
NC 10	11 NC

NC – No internal connection

TLC070, TLC071, TLC072, TLC073, TLC074, TLC075, TLC07xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	17 V
Differential input voltage, V_{ID}	$\pm V_{DD}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DGN (8)	4.7	52.7	2.37 W
DGQ (10)	4.7	52.3	2.39 W
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PWP (20)	1.40	26.1	4.79 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	4.5	16	V
	Split supply	±2.25	±8	
Common-mode input voltage range, V_{ICR}		+0.5	V_{DD}−0.8	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	−40	125	

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5, V_O = 2.5, R_S = 50 Ω	TLC070/1/2/3	25°C		60	1000	μV
				Full range			1500	
			TLC070/1/2/3A	25°C		20	750	
				Full range			1000	
			TLC074/5	25°C		390	1900	
				Full range			3000	
			TLC074/5A	25°C		390	1400	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage					1.2		μV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5, V_O = 2.5, R_S = 50 Ω		25°C		0.7	50	pA
			TLC07XC	Full range			100	
			TLC07XI				700	
I_{IB}	Input bias current			25°C		1.5	50	pA
			TLC07XC	Full range			100	
			TLC07XI				700	
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB,	R_S = 50 Ω	25°C	0.5 to 4.2			V
		CMRR > 52 dB,	R_S = 50 Ω	Full range	0.5 to 4.2			
V_{OH}	High-level output voltage	V_{IC} = 2.5 V	I_{OH} = −1 mA	25°C	4.1	4.3		V
				Full range	3.9			
			I_{OH} = −20 mA	25°C	3.7	4		
				Full range	3.5			
			I_{OH} = −35 mA	25°C	3.4	3.8		
				Full range	3.2			
			I_{OH} = −50 mA	25°C	3.2	3.6		
				−40°C to 85°C	3			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 1 mA	25°C		0.18	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.39	
				Full range			0.45	
			I_{OL} = 35 mA	25°C		0.43	0.55	
				Full range			0.7	
			I_{OL} = 50 mA	25°C		0.48	0.63	
				−40°C to 85°C			0.7	
I_{OS}	Short-circuit output current	Sourcing		25°C		100		mA
		Sinking		25°C		100		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail		25°C		55		

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 3 V,	R_L = 10 kΩ	25°C	100	120		dB
				Full range	100			
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		22.9		pF
z_O	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 1 to 3 V,	R_S = 50 Ω	25°C	100	140		dB
				Full range	100			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.5 V to 16 V, No load	V_{IC} = V_{DD}/2,	25°C	95	130		dB
				Full range	95			
I_{DD}	Supply current (per channel)	V_O = 2.5 V,	No load	25°C		1.9	2.5	mA
				Full range			3.5	
$V_{(ON)}$	Turnon voltage level	Relative to GND		25°C		1.41		V
$V_{(OFF)}$	Turnoff voltage level	Relative to GND		25°C		1.4		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (per channel) (TLC070, TLC073, TLC075)	SHDN ≤ 1.45 V		25°C		125	200	μA
				Full range			250	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	10	16		V/µs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	12.5	19		V/µs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		12		nV/√Hz
		f = 1 kHz		25°C		7		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002%		
			A_V = 10			0.012%		
			A_V = 100			0.085%		
$t_{(on)}$	Amplifier turnon time‡	R_L = 10 kΩ		25°C		0.15		µs
$t_{(off)}$	Amplifier turnoff time‡			25°C		1.3		µs
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		10		MHz
t_S	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.18		µs
			0.01%			0.39		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.18		
			0.01%			0.39		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		32°		
		R_L = 10 kΩ,	C_L = 0 pF			40°		
	Gain margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		2.2		dB
		R_L = 10 kΩ,	C_L = 0 pF			3.3		

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.
‡ Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

electrical characteristics at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 12 V, V_{IC} = 6, V_O = 6, R_S = 50 Ω	TLC070/1/2/3	25°C		60	1000	µV
				Full range			1500	
			TLC070/1/2/3A	25°C		20	750	
				Full range			1000	
			TLC074/5	25°C		390	1900	
				Full range			3000	
			TLC074/5A	25°C		390	1400	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage					1.2		µV/°C
I_{IO}	Input offset current	V_{DD} = 12 V, V_{IC} = 6, V_O = 6, R_S = 50 Ω		25°C		0.7	50	pA
			TLC07xC	Full range			100	
			TLC07xI				700	
I_{IB}	Input bias current			25°C		1.5	50	pA
			TLC07xC	Full range			100	
			TLC07xI				700	
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB	R_S = 50 Ω	25°C	0.5 to 11.2			V
		CMRR > 52 dB	R_S = 50 Ω	Full range	0.5 to 11.2			
V_{OH}	High-level output voltage	V_{IC} = 6 V	I_{OH} = −1 mA	25°C	11.1	11.2		V
				Full range	11			
			I_{OH} = −20 mA	25°C	10.8	10.9		
				Full range	10.7			
			I_{OH} = −35 mA	25°C	10.6	10.7		
				Full range	10.3			
			I_{OH} = −50 mA	25°C	10.4	10.5		
				−40°C to 85°C	10.3			
V_{OL}	Low-level output voltage	V_{IC} = 6 V	I_{OL} = 1 mA	25°C		0.17	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.45	
				Full range			0.5	
			I_{OL} = 35 mA	25°C		0.4	0.52	
				Full range			0.6	
			I_{OL} = 50 mA	25°C		0.45	0.6	
				−40°C to 85°C			0.65	
I_{OS}	Short-circuit output current	Sourcing		25°C		150		mA
		Sinking		25°C		150		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail		25°C		55		

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted) (continued)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 8 V,	R_L = 10 kΩ	25°C	120	140		dB
				Full range	120			
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		21.6		pF
z_O	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 1 to 10 V,	R_S = 50 Ω	25°C	100	140		dB
				Full range	100			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.5 V to 16 V, No load	V_{IC} = V_{DD}/2,	25°C	95	130		dB
				Full range	95			
I_{DD}	Supply current (per channel)	V_O = 7.5 V,	No load	25°C		2.1	2.9	mA
				Full range			3.5	
$V_{(ON)}$	Turnon voltage level	Relative to GND		25°C		1.39		V
$V_{(OFF)}$	Turnoff voltage level	Relative to GND		25°C		1.38		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLC070, TLC073, TLC075) (per channel)	$\overline{SHDN}$ ≤ 1.45 V		25°C		125	200	µA
				Full range			250	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 50 pF, R_L = 10 kΩ		25°C	10	16		V/µs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 50 pF, R_L = 10 kΩ		25°C	12.5	19		V/µs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		12		nV/√Hz
		f = 1 kHz		25°C		7		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 8 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002%		
			A_V = 10			0.005%		
			A_V = 100			0.022%		
$t_{(on)}$	Amplifier turnon time‡	R_L = 10 kΩ		25°C		0.47		µs
$t_{(off)}$	Amplifier turnoff time‡			25°C		2.5		µs
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		10		MHz
t_S	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.17		µs
			0.01%			0.22		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.17		
			0.01%			0.29		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		37°		
		R_L = 10 kΩ,	C_L = 0 pF			42°		
	Gain margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		3.1		dB
		R_L = 10 kΩ,	C_L = 0 pF			4		

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.
‡ Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.
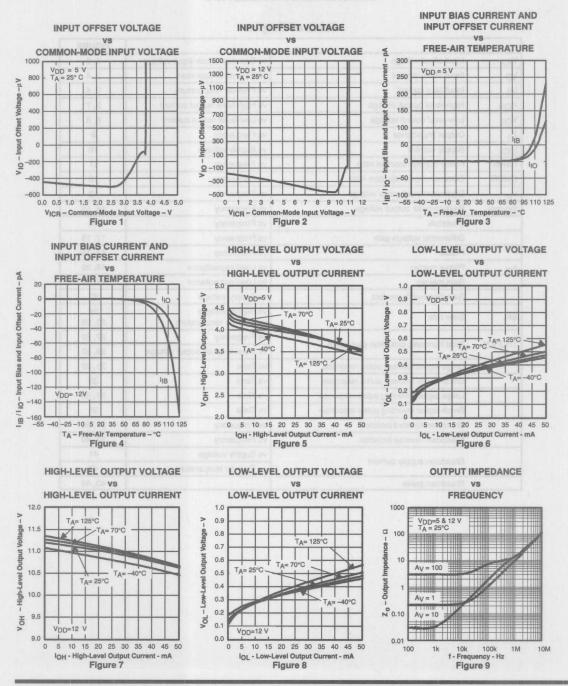
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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
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I_{IO}	Input offset current	vs Free-air temperature	3, 4
I_{IB}	Input bias current	vs Free-air temperature	3, 4
V_{OH}	High-level output voltage	vs High-level output current	5, 7
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8
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PSRR	Power supply rejection ratio	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
V_n	Equivalent input noise voltage	vs Frequency	13
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	Differential voltage gain	vs Frequency	17, 18
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	Gain-bandwidth product	vs Supply voltage	23
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	Shutdown supply current	vs Supply voltage	41
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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 2

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

Figure 3

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 8

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 9

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TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 10

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

Figure 11

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 12

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 13

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 14

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 15

CROSSTALK
vs
FREQUENCY

Figure 16

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TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE GAIN AND
PHASE
vs
FREQUENCY

Figure 17

DIFFERENTIAL VOLTAGE GAIN AND
PHASE
vs
FREQUENCY

Figure 18

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 19

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 20

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 21

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 22

GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

Figure 23

SLEW RATE
vs
SUPPLY VOLTAGE

Figure 24

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TYPICAL CHARACTERISTICS

**SLEW RATE
vs
FREE-AIR TEMPERATURE**

V_{DD} = 5 V
R_L = 600 Ω & 10 kΩ
C_L = 50pF
A_V = 1

Figure 25

**SLEW RATE
vs
FREE-AIR TEMPERATURE**

V_{DD} = 12 V
R_L = 600 Ω & 10 kΩ
C_L = 50pF
A_V = 1

Figure 26

**TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
FREQUENCY**

V_{DD} = 5 V
R_L = 10 kΩ
$V_{O(PP)}$ = 2 V

Figure 27

**TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
FREQUENCY**

V_{DD} = 12 V
R_L = 10 kΩ
$V_{O(PP)}$ = 12 V

Figure 28

**TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
PEAK-TO-PEAK OUTPUT VOLTAGE**

V_{DD} = 5 V
A_V = 1
f = 1 kHz

Figure 29

**TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
PEAK-TO-PEAK OUTPUT VOLTAGE**

V_{DD} = 12 V
A_V = 1
f = 1 kHz

Figure 30

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME**

V_{DD} = 5 V
R_L = 600 Ω
& 10 kΩ
C_L = 8 pF
T_A = 25°C

Figure 31

**LARGE SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME**

V_{DD} = 12 V
R_L = 600 Ω
& 10 kΩ
C_L = 8 pF
T_A = 25°C

Figure 32

**SMALL SIGNAL FOLLOWER PULSE
RESPONSE
vs
TIME**

V_{DD} = 5 &12V
R_L = 600 Ω & 10 kΩ
C_L = 8 pF
T_A = 25°C

Figure 33

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TYPICAL CHARACTERISTICS

**LARGE SIGNAL INVERTING
PULSE RESPONSE
vs
TIME**

Figure 34

**LARGE SIGNAL INVERTING
PULSE RESPONSE
vs
TIME**

Figure 35

**SMALL SIGNAL INVERTING
PULSE RESPONSE
vs
TIME**

Figure 36

**SHUTDOWN FORWARD
ISOLATION
vs
FREQUENCY**

Figure 37

**SHUTDOWN FORWARD
ISOLATION
vs
FREQUENCY**

Figure 38

**SHUTDOWN REVERSE
ISOLATION
vs
FREQUENCY**

Figure 39

**SHUTDOWN REVERSE
ISOLATION
vs
FREQUENCY**

Figure 40

**SHUTDOWN SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

Figure 41

**SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE**

Figure 42

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TYPICAL CHARACTERISTICS

SHUTDOWN PULSE

Figure 43

SHUTDOWN PULSE

Figure 44

PARAMETER MEASUREMENT INFORMATION

Figure 45

APPLICATION INFORMATION

input offset voltage null circuit

The TLC070 and TLC071 has an input offset nulling function. Refer to Figure 46 for the diagram.

NOTE A. If R1 = 5.6 kΩ for offset voltage adjustment of ±10 mV.
         If R1 = 20 kΩ for offset voltage adjustment of ±3 mV.

Figure 46. Input Offset Voltage Null Circuit

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APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 47. A minimum value of 20 Ω should work well for most applications.

Figure 47. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 48. Output Offset Voltage Model

APPLICATION INFORMATION

high speed CMOS input amplifiers

The TLC07x is a family of high-speed low-noise CMOS input operational amplifiers and has an input capacitance of the order of 20 pF. Any resistor used in the feedback path adds a pole in the transfer function equivalent to the input capacitance multiplied by the combination of source resistance and feedback resistance. For example, a gain of –10, source resistance of 1 kΩ and a feedback resistance of 10 kΩ adds an additional pole at approximately 8 MHz. This is more apparent with CMOS amplifiers than bipolar amplifiers due to their greater input capacitance.

This is of little consequence on slower CMOS amplifiers, as this pole normally occurs at frequencies above their unity-gain bandwidth. However, the TLC07x with its 10-MHz bandwidth means that this pole normally occurs at frequencies where there is on the order of 5 dB gain left and the phase shift adds considerably.

The effect of this pole is the strongest with large feedback resistances at small closed loop gains. As the feedback resistance is increased, the gain peaking increases at a lower frequency and the 180° phase shift crossover point also moves down in frequency, decreasing the phase margin.

For the TLC07x, the maximum feedback resistor recommended is 5 kΩ, larger resistances can be used but a capacitor in parallel with the feedback resistor is recommended to counter the effects of the input capacitance pole.

The TLC073 with a 1-V step response has an 80% overshoot with a natural frequency of 3.5 MHz when configured as a unity gain buffer and with a 10-kΩ feedback resistor. By adding a 10-pF capacitor in parallel with the feedback resistor, the overshoot is reduced to 40% and eliminates the natural frequency, resulting in a much faster settling time (see Figure 49). The 10-pF capacitor was chosen for convenience only.

Load capacitance had little effect on these measurements due to the excellent output drive capability of the TLC07x.
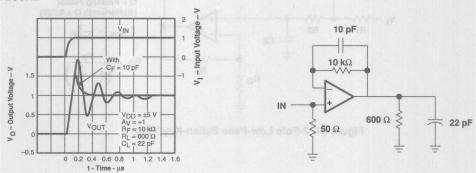
Figure 49. 1-V Step Response

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 50).
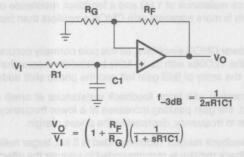
$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 50. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 51. 2-Pole Low-Pass Sallen-Key Filter

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APPLICATION INFORMATION

shutdown function

Three members of the TLC07x family (TLC070/3/5) have a shutdown terminal ($\overline{\text{SHDN}}$) for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 16 nA/channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 43 and 44. The amplifier is powered with a single 5-V supply and is configured as noninverting with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 37, 38, 39, and 40 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency using 0.1 V_{PP}, 2.5 V_{PP}, and 5 V_{PP} input signals at ±2.5 V supplies and 0.1 V_{PP}, 8 V_{PP}, and 12 V_{PP} input signals at ±6 V supplies.

circuit layout considerations

To achieve the levels of high performance of the TLC07x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.

- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.

- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.
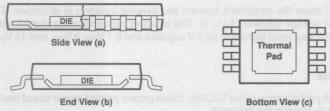
APPLICATION INFORMATION

general PowerPAD™ design considerations

The TLC07x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 52(a) and Figure 52(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 52(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

Side View (a)

End View (b)

Bottom View (c)

NOTE B. The thermal pad is electrically isolated from all terminals in the package.

Figure 52. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

Thermal Pad Area

Single or Dual

68 mils x 70 mils) with 5 vias
(Via diameter = 13 mils

Quad

78 mils x 94 mils) with 9 vias
(Via diameter = 13 mils)

Figure 53. PowerPAD PCB Etch and Via Pattern

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APPLICATION INFORMATION

general PowerPAD design considerations (continued)

1. Prepare the PCB with a top side etch pattern as shown in Figure 53. There should be etch for the leads as well as etch for the thermal pad.

2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLC07x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.

4. Connect all holes to the internal ground plane.

5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLC07x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the TLC07x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 54 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLC07x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
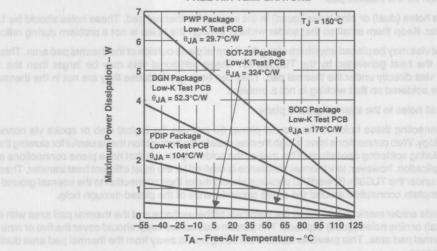θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

NOTE A.   Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 54. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially muti-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 55 are generated using the TLC07x typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).

APPLICATION INFORMATION


```
*DEVICE=TLC07X,OPAMP,NPN,INT
* TLC07X operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 06/21/99 at 17:12
* Parts is a MicroSim product.
*
* connections:   non–inverting input
*                  inverting input
*                    positive power supply
*                     negative power supply
*                      output
*
.subckt TLC07X–X 1 2 3 4 5
*
  c1   11 12 4.8697E–12
  c2   6  7 8.0000E–12
  cee  10 99 4.0063E–12
  dc   5 53 dy
  de   54 5 dy
  dlp  90 91 dx
  dln  92 90 dx
  dp   4 3 dx
  egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
  fb   7 99 poly(5) vb vc ve vlp vln 0 6.9134E6 –1E3 1E3
+6E6 –6E6
  ga   6 0 11 12 457.42E–6
  gcm  0 6 10 99 1.1293E–6
```

```
  iee  10 4 dc 183.67E–6
  ioff 0 6 dc .95E–6
  hlim 90 0 vlim 1K
  q1   11 2 13 qx1
  q2   12 1 14 qx2
  r2   6 9 100.00E3
  rc1  3 11 2.1862E3
  rc2  3 12 2.1862E3
  re1  13 10 1.9046E3
  re2  14 10 1.9046E3
  ree  10 99 1.0889E6
  ro1  8 5 10
  ro2  7 99 10
  rp   3 4 2.7199E3
  vb   9 0 dc 0
  vc   3 53 dc 1.5410
  ve   54 4 dc .84403
  vlim 7 8 dc 0
  vlp  91 0 dc 119
  vln  0 92 dc 119
  .model dx D(Is=800.00E–18)
  .model dy D(Is=800.00E–18 Rs=1m Cjo=10p)
  .model qx1 NPN(Is=800.00E–18 Bf=390.79E6)
  .model qx2 NPN(Is=800.0000E–18 Bf=390.79E6)
  .ends
*$
```

Figure 55. Boyle Macromodel and Subcircuit

TLC080, TLC081, TLC082, TLC083, TLC084, TLC085, TLC08xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY OPERATIONAL AMPLIFIERS

- **Wide Bandwidth . . . 10 MHz**
- **High Output Drive**
  - I_{OH} . . . 57 mA at V_{DD} – 1.5
  - I_{OL} . . . 55 mA at 0.5 V
- **High Slew Rate**
  - SR+ . . . 16 V/μs
  - SR– . . . 19 V/μs
- **Wide Supply Range . . . 4.5 V to 16 V**
- **Supply Current . . . 1.9 mA/Channel**
- **Ultra-Low Power Shutdown Mode**
  I_{DD} . . . 125 μA/Channel
- **Low Input Noise Voltage . . . 8.5 nV$\sqrt{Hz}$**
- **Wide V_{ICR} . . . 0 to V_{DD} – 1**
- **Input Offset Voltage . . . 60 μV**
- **Ultra-Small Packages**
  - 8 or 10 Pin MSOP (TLC080/1/2/3)

TLC080
D, DGN OR P PACKAGE
(TOP VIEW)

NULL	1	8	$\overline{SHDN}$
IN–	2	7	V_{DD}
IN+	3	6	OUT
GND	4	5	NULL

description

Introducing the first members of TI's new BiMOS general-purpose operational amplifier family—the TLC08x. The BiMOS family concept is simple: provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher ac and dc performance. With performance rated from 4.5 V to 16 V across commercial (0°C to 70°C) and an extended industrial temperature range (–40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial and instrumentation applications. Familiar features like offset nulling pins, and new features like MSOP PowerPAD™ packages and shutdown modes, enable higher levels of performance in a multitude of applications.

Developed in TI's patented LBC3 BiCMOS process, the new BiMOS amplifiers combine a very high input impedance, low-noise CMOS front end with a high-drive Bipolar output stage—thus providing the optimum performance features of both. AC performance improvements over the TL08x BiFET predecessors include a bandwidth of 10 MHz (an increase of 300%) and voltage noise of 8.5 nV/$\sqrt{Hz}$ (an improvement of 60%). DC improvements include an ensured V_{ICR} that includes ground, a factor of 4 reduction in input offset voltage down to 1.5 mV (maximum) in the standard grade, and a power supply rejection improvement of greater than 40 dB to 130 dB. Added to this list of impressive features is the ability to drive ±50-mA loads comfortably from an ultra-small-footprint MSOP PowerPAD package, which positions the TLC08x as the ideal high-performance general-purpose operational amplifier family.

FAMILY PACKAGE TABLE

DEVICE	NO. OF CHANNELS	PACKAGE TYPES				SHUTDOWN	UNIVERSAL EVM BOARD
		MSOP	PDIP	SOIC	TSSOP		
TLC080	1	8	8	8	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLC081	1	8	8	8	—		
TLC082	2	8	8	8	—	—	
TLC083	2	10	14	14	—	Yes	
TLC084	4	—	14	14	20	—	
TLC085	4	—	16	16	20	Yes	

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**TEXAS INSTRUMENTS**

TLC080 and TLC081 AVAILABLE OPTIONS

| T_A | PACKAGED DEVICES | PACKAGED DEVICES | | |
	SMALL OUTLINE (D)†	SMALL OUTLINE (DGN)†	SYMBOL	PLASTIC DIP (P)
0°C to 70°C	TLC080CD TLC081CD	TLC080CDGN TLC081CDGN	xxTIACW xxTIACY	TLC080CP TLC081CP
−40°C to 125°C	TLC080ID TLC081ID	TLC080IDGN TLC081IDGN	xxTIACX xxTIACZ	TLC080IP TLC081IP
	TLC080AID TLC081AID	— —	— —	TLC080AIP TLC081AIP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC080CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLC082 and TLC083 AVAILABLE OPTIONS

| T_A | PACKAGED DEVICES | | | | | | |
| | SMALL OUTLINE (D)† | MSOP | | | | PLASTIC DIP (N) | PLASTIC DIP (P) |
		(DGN)†	SYMBOL§	(DGQ)†	SYMBOL§		
0°C to 70°C	TLC082CD TLC083CD	TLC082CDGN —	xxTIADZ —	— TLC083CDGQ	— xxTIAEB	— TLC083CN	TLC082CP —
−40°C to 125°C	TLC082ID TLC083ID	TLC082IDGN —	xxTIAEA —	— TLC083IDGQ	— xxTIAEC	— TLC083IN	TLC082IP —
	TLC082AID TLC083AID	— —	— —	— —	— —	— TLC083AIN	TLC082AIP —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC082CDR).
‡ Chip forms are tested at T_A = 25°C only.
§ xx represents the device date code.

TLC084 and TLC085 AVAILABLE OPTIONS

| T_A | PACKAGED DEVICES | | |
	SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PWP)†
0°C to 70°C	TLC084CD TLC085CD	TLC084CN TLC085CN	TLC084CPWP TLC085CPWP
−40°C to 125°C	TLC084ID TLC085ID	TLC084IN TLC085IN	TLC084IPWP TLC085IPWP
	TLC084AID TLC085AID	TLC084AIN TLC085AIN	TLC084AIPWP TLC085AIPWP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLC084CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLC08x PACKAGE PINOUTS

TLC080
D, DGN OR P PACKAGE
(TOP VIEW)

NULL	1	8	SHDN
IN–	2	7	V$_{DD}$
IN+	3	6	OUT
GND	4	5	NULL

TLC081
D, DGN OR P PACKAGE
(TOP VIEW)

NULL	1	8	NC
IN–	2	7	V$_{DD}$
IN+	3	6	OUT
GND	4	5	NULL

TLC082
D, DGN, OR P PACKAGE
(TOP VIEW)

1OUT	1	8	V$_{DD}$
1IN–	2	7	2OUT
1IN+	3	6	2IN–
GND	4	5	2IN+

TLC083
DGQ PACKAGE
(TOP VIEW)

1OUT	1	10	V$_{DD}$
1IN–	2	9	2OUT
1IN+	3	8	2IN–
GND	4	7	2IN+
1SHDN	5	6	2SHDN

TLC083
D OR N PACKAGE
(TOP VIEW)

1OUT	1	14	V$_{DD}$
1IN–	2	13	2OUT
1IN+	3	12	2IN–
GND	4	11	2IN+
NC	5	10	NC
1SHDN	6	9	2SHDN
NC	7	8	NC

TLC084
D OR N PACKAGE
(TOP VIEW)

1OUT	1	14	4OUT
1IN–	2	13	4IN–
1IN+	3	12	4IN+
V$_{DD}$	4	11	GND
2IN+	5	10	3IN+
2IN–	6	9	3IN–
2OUT	7	8	3OUT

TLC084
PWP PACKAGE
(TOP VIEW)

1OUT	1	20	4OUT
1IN–	2	19	4IN–
1IN+	3	18	4IN+
VDD	4	17	GND
2IN+	5	16	3IN+
2IN–	6	15	3IN–
2OUT	7	14	3OUT
NC	8	13	NC
NC	9	12	NC
NC	10	11	NC

TLC085
D OR N PACKAGE
(TOP VIEW)

1OUT	1	16	4OUT
1IN–	2	15	4IN–
1IN+	3	14	4IN+
V$_{DD}$	4	13	GND
2IN+	5	12	3IN+
2IN–	6	11	3IN–
2OUT	7	10	3OUT
1/2SHDN	8	9	3/4SHDN

TLC085
PWP PACKAGE
(TOP VIEW)

1OUT	1	20	4OUT
1IN–	2	19	4IN–
1IN+	3	18	4IN+
VDD	4	17	GND
2IN+	5	16	3IN+
2IN–	6	15	3IN–
2OUT	7	14	3OUT
1/2SHDN	8	13	3/4SHDN
NC	9	12	NC
NC	10	11	NC

NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	17 V
Differential input voltage, V_{ID}	$\pm V_{DD}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix	0°C to 70°C
I suffix	−40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25$°C POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DGN (8)	4.7	52.7	2.37 W
DGQ (10)	4.7	52.3	2.39 W
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PWP (20)	1.40	26.1	4.79 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	4.5	16	V
	Split supply	±2.25	±8	
Common-mode input voltage range, V_{ICR}		GND	$V_{DD}-1$	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	−40	125	

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5, V_O = 2.5, R_S = 50 Ω	TLC080/1/2/3	25°C		60	1000	µV
				Full range			1500	
			TLC080/1/2/3A	25°C		20	750	
				Full range			1000	
			TLC084/5	25°C		390	1900	
				Full range			3000	
			TLC084/5A	25°C		390	1400	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage					1.2		µV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5, V_O = 2.5, R_S = 50 Ω		25°C		1.9	50	pA
			TLC08XC	Full range			100	
			TLC08XI				700	
I_{IB}	Input bias current			25°C		3	50	pA
			TLC08XC	Full range			100	
			TLC08XI				700	
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB,	R_S = 50 Ω	25°C	0 to 3.5			V
		CMRR > 52 dB,	R_S = 50 Ω	Full range	0 to 3.5			
V_{OH}	High-level output voltage	V_{IC} = 2.5 V	I_{OH} = −1 mA	25°C	4.1	4.3		V
				Full range	3.9			
			I_{OH} = −20 mA	25°C	3.7	4		
				Full range	3.5			
			I_{OH} = −35 mA	25°C	3.4	3.8		
				Full range	3.2			
			I_{OH} = −50 mA	25°C	3.2	3.6		
				−40°C to 85°C	3			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 1 mA	25°C		0.18	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.39	
				Full range			0.45	
			I_{OL} = 35 mA	25°C		0.43	0.55	
				Full range			0.7	
			I_{OL} = 50 mA	25°C		0.45	0.63	
				−40°C to 85°C			0.7	
I_{OS}	Short-circuit output current	Sourcing		25°C		100		mA
		Sinking		25°C		100		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail		25°C		55		

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 3 V,	R_L = 10 kΩ	25°C	100	120		dB
				Full range	100			
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		22.9		pF
z_O	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3 V,	R_S = 50 Ω	25°C	100	140		dB
				Full range	100			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 4.5 V to 16 V, No load	V_{IC} = V_{DD}/2,	25°C	95	130		dB
				Full range	95			
I_{DD}	Supply current (per channel)	V_O = 2.5 V,	No load	25°C		1.8	2.5	mA
				Full range			3.5	
$V_{(ON)}$	Turnon voltage level	Relative to GND		25°C		1.41		V
$V_{(OFF)}$	Turnoff voltage level	Relative to GND		25°C		1.4		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (per channel) (TLC080, TLC083, TLC085)	$\overline{SHDN}$ ≤ 1.45 V		25°C		125	200	µA
				Full range			250	

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.

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operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	10	16		V/μs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	12.5	19		V/μs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C			12	nV/√Hz
		f = 1 kHz		25°C			8.5	
I_n	Equivalent input noise current	f = 1 kHz		25°C			0.6	fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002%		
			A_V = 10			0.012%		
			A_V = 100			0.085%		
$t_{(on)}$	Amplifier turnon time‡	R_L = 10 kΩ		25°C		0.15		μs
$t_{(off)}$	Amplifier turnoff time‡			25°C		1.3		μs
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		10		MHz
t_S	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.18		μs
			0.01%			0.39		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.18		
			0.01%			0.39		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		32°		
		R_L = 10 kΩ,	C_L = 0 pF			40°		
	Gain margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		2.2		dB
		R_L = 10 kΩ,	C_L = 0 pF			3.3		

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.
‡ Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

electrical characteristics at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD} = 12$ V $V_{IC} = 6$, $V_O = 6$, $R_S = 50 \Omega$	TLC080/1/2/3	25°C		60	1000	µV
				Full range			1500	
			TLC080/1/2/3A	25°C		20	750	
				Full range			1000	
			TLC084/5	25°C		390	1900	
				Full range			3000	
			TLC084/5A	25°C		390	1400	
				Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage					1.2		µV/°C
I_{IO}	Input offset current	$V_{DD} = 12$ V $V_{IC} = 6$, $V_O = 6$, $R_S = 50 \Omega$		25°C		1.5	50	pA
			TLC08xC	Full range			100	
			TLC08xI				700	
I_{IB}	Input bias current			25°C		2	50	pA
			TLC08xC	Full range			100	
			TLC08xI				700	
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB	$R_S = 50 \Omega$	25°C	0 to 10.5			V
		CMRR > 52 dB	$R_S = 50 \Omega$	Full range	0 to 10.5			
V_{OH}	High-level output voltage	$V_{IC} = 6$ V	$I_{OH} = -1$ mA	25°C	11.1	11.2		V
				Full range	11			
			$I_{OH} = -20$ mA	25°C	10.8	11		
				Full range	10.7			
			$I_{OH} = -35$ mA	25°C	10.6	10.7		
				Full range	10.3			
			$I_{OH} = -50$ mA	25°C	10.3	10.5		
				−40°C to 85°C	10.2			
V_{OL}	Low-level output voltage	$V_{IC} = 6$ V	$I_{OL} = 1$ mA	25°C		0.17	0.25	V
				Full range			0.35	
			$I_{OL} = 20$ mA	25°C		0.35	0.45	
				Full range			0.5	
			$I_{OL} = 35$ mA	25°C		0.4	0.52	
				Full range			0.6	
			$I_{OL} = 50$ mA	25°C		0.45	0.6	
				−40°C to 85°C			0.65	
I_{OS}	Short-circuit output current	Sourcing		25°C		150		mA
		Sinking		25°C		150		
I_O	Output current	$V_{OH} = 1.5$ V from positive rail		25°C		57		mA
		$V_{OL} = 0.5$ V from negative rail		25°C		55		

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

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electrical characteristics at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 8 V,	R_L = 10 kΩ	25°C	120	140		dB
				Full range	120			
$r_{i(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		21.6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 10 V,	R_S = 50 Ω	25°C	100	140		dB
				Full range	100			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 4.5 V to 16 V, No load	V_{IC} = V_{DD}/2,	25°C	95	130		dB
				Full range	95			
I_{DD}	Supply current (per channel)	V_O = 7.5 V,	No load	25°C		1.9	2.9	mA
				Full range			3.5	
$V_{(ON)}$	Turnon voltage level	Relative to GND		25°C		1.39		V
$V_{(OFF)}$	Turnoff voltage level	Relative to GND		25°C		1.38		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLC080, TLC083, TLC085) (per channel)	$\overline{SHDN}$ ≤ 1.45 V		25°C		125	200	μA
				Full range			250	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 12 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	10	16		V/μs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 50 pF,	25°C	12.5	19		V/μs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz		25°C		8.5		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 8 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002%		
			A_V = 10			0.005%		
			A_V = 100			0.022%		
$t_{(on)}$	Amplifier turnon time‡	R_L = 10 kΩ		25°C		0.47		μs
$t_{(off)}$	Amplifier turnoff time‡			25°C		2.5		μs
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		10		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.17		μs
			0.01%			0.22		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.17		
			0.01%			0.29		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		37°		
		R_L = 10 kΩ,	C_L = 0 pF			42°		
	Gain margin	R_L = 10 kΩ,	C_L = 50 pF	25°C		3.1		dB
		R_L = 10 kΩ,	C_L = 0 pF			4		

† Full range is 0°C to 70°C for C suffix and –40°C to 125°C for I suffix. If not specified, full range is –40°C to 125°C.
‡ Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

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TYPICAL CHARACTERISTICS

Table of Graphs

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I_{IO}	Input offset current	vs Free-air temperature	3, 4
I_{IB}	Input bias current	vs Free-air temperature	3, 4
V_{OH}	High-level output voltage	vs High-level output current	5, 7
V_{OL}	Low-level output voltage	vs Low-level output current	6, 8
Z_o	Output impedance	vs Frequency	9
I_{DD}	Supply current	vs Supply voltage	10
PSRR	Power supply rejection ratio	vs Frequency	11
CMRR	Common-mode rejection ratio	vs Frequency	12
V_n	Equivalent input noise voltage	vs Frequency	13
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	14, 15
	Crosstalk	vs Frequency	16
	Differential voltage gain	vs Frequency	17, 18
	Phase	vs Frequency	17, 18
ϕ_m	Phase margin	vs Load capacitance	19, 20
	Gain margin	vs Load capacitance	21, 22
	Gain-bandwidth product	vs Supply voltage	23
SR	Slew rate	vs Supply voltage	24
		vs Free-air temperature	25, 26
THD + N	Total harmonic distortion plus noise	vs Frequency	27, 28
		vs Peak-to-peak output voltage	29, 30
	Large-signal follower pulse response	vs Time	31, 32
	Small-signal follower pulse response	vs Time	33
	Large-signal inverting pulse response	vs Time	34, 35
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TLC080, TLC081, TLC082, TLC083, TLC084, TLC085, TLC08xA
FAMILY OF WIDE-BANDWIDTH HIGH-OUTPUT-DRIVE SINGLE SUPPLY
OPERATIONAL AMPLIFIERS

SLOS254B – JUNE 1999 – REVISED NOVEMBER 1999

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 2

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

Figure 3

INPUT BIAS CURRENT AND
INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

Figure 4

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 5

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 8

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 9

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 10

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

Figure 11

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 12

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 13

PEAK-TO-PEAK OUTPUT
VOLTAGE
vs
FREQUENCY

Figure 14

PEAK-TO-PEAK OUTPUT
VOLTAGE
vs
FREQUENCY

Figure 15

CROSSTALK
vs
FREQUENCY

Figure 16

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TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE GAIN AND
PHASE
vs
FREQUENCY

Figure 17

DIFFERENTIAL VOLTAGE GAIN AND
PHASE
vs
FREQUENCY

Figure 18

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 19

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 20

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 21

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 22

GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

Figure 23

SLEW RATE
vs
SUPPLY VOLTAGE

Figure 24

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TYPICAL CHARACTERISTICS

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 25

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 26

TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
FREQUENCY

Figure 27

TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
FREQUENCY

Figure 28

TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

Figure 29

TOTAL HARMONIC DISTORTION
PLUS NOISE
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

Figure 30

LARGE SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME

Figure 31

LARGE SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME

Figure 32

SMALL SIGNAL FOLLOWER PULSE
RESPONSE
vs
TIME

Figure 33

TYPICAL CHARACTERISTICS

LARGE SIGNAL INVERTING PULSE RESPONSE vs TIME

V_I (2 V/div)
V_{DD} = 5 V
R_L = 600 Ω & 10 kΩ
C_L = 8 pF
T_A = 25°C
V_O (500 mV/Div)

Figure 34

LARGE SIGNAL INVERTING PULSE RESPONSE vs TIME

V_I (5 V/div)
V_{DD} = 12 V
R_L = 600 Ω & 10 kΩ
C_L = 8 pF
T_A = 25°C
V_O (2 V/Div)

Figure 35

SMALL SIGNAL INVERTING PULSE RESPONSE vs TIME

V_I (100 mV/div)
V_{DD} = 5 & 12 V
R_L = 600 Ω & 10 kΩ
C_L = 8 pF
T_A = 25°C
V_O (50 mV/Div)

Figure 36

SHUTDOWN FORWARD ISOLATION vs FREQUENCY

V_{DD} = 5 V
C_L = 0 pF
T_A = 25°C
$V_{I(PP)}$ = 0.1, 2.5, and 5
R_L = 600 Ω
R_L = 10 kΩ

Figure 37

SHUTDOWN FORWARD ISOLATION vs FREQUENCY

V_{DD} = 12 V
C_L = 0 pF
T_A = 25°C
$V_{I(PP)}$ = 0.1, 8, 12
R_L = 600 Ω
R_L = 10 kΩ

Figure 38

SHUTDOWN REVERSE ISOLATION vs FREQUENCY

V_{DD} = 5 V
C_L = 0 pF
T_A = 25°C
$V_{I(PP)}$ = 0.1, 2.5, and 5
R_L = 600 Ω
R_L = 10 kΩ

Figure 39

SHUTDOWN REVERSE ISOLATION vs FREQUENCY

V_{DD} = 12 V
C_L = 0 pF
T_A = 25°C
$V_{I(PP)}$ = 0.1, 8, 12
R_L = 600 Ω
R_L = 10 kΩ

Figure 40

SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE

Shutdown On
R_L = open
V_{IN} = V_{DD}/2

Figure 41

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

A_V = 1
V_{IN} = V_{DD}/2
V_{DD} = 12 V
V_{DD} = 5 V

Figure 42

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TYPICAL CHARACTERISTICS

SHUTDOWN PULSE

$V_{DD} = 5$ V
$C_L = 8$ pF
$T_A = 25°C$

I_{DD} $R_L = 10$ kΩ

I_{DD} $R_L = 600$ Ω

Figure 43

SHUTDOWN PULSE

$V_{DD} = 12$ V
$C_L = 8$ pF
$T_A = 25°C$

I_{DD} $R_L = 10$ kΩ

I_{DD} $R_L = 600$ Ω

Figure 44

PARAMETER MEASUREMENT INFORMATION

Figure 45

APPLICATION INFORMATION

input offset voltage null circuit

The TLC080 and TLC081 has an input offset nulling function. Refer to Figure 46 for the diagram.

NOTE A. If R1 = 5.6 kΩ for offset voltage adjustment of ±10 mV.
If R1 = 20 kΩ for offset voltage adjustment of ±3 mV.

Figure 46. Input Offset Voltage Null Circuit

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APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 47. A minimum value of 20 Ω should work well for most applications.

Figure 47. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 48. Output Offset Voltage Model

APPLICATION INFORMATION

high speed CMOS input amplifiers

The TLC08x is a family of high-speed low-noise CMOS input operational amplifiers and has an input capacitance of the order of 20 pF. Any resistor used in the feedback path adds a pole in the transfer function equivalent to the input capacitance multiplied by the combination of source resistance and feedback resistance. For example, a gain of –10, source resistance of 1 kΩ and a feedback resistance of 10 kΩ adds an additional pole at approximately 8 MHz. This is more apparent with CMOS amplifiers than bipolar amplifiers due to their greater input capacitance.

This is of little consequence on slower CMOS amplifiers, as this pole normally occurs at frequencies above their unity-gain bandwidth. However, the TLC08x with its 10-MHz bandwidth means that this pole normally occurs at frequencies where there is on the order of 5dB gain left and the phase shift adds considerably.

The effect of this pole is the strongest with large feedback resistances at small closed loop gains. As the feedback resistance is increased, the gain peaking increases at a lower frequency and the 180° phase shift crossover point also moves down in frequency, decreasing the phase margin.

For the TLC08x, the maximum feedback resistor recommended is 5 kΩ, larger resistances can be used but a capacitor in parallel with the feedback resistor is recommended to counter the effects of the input capacitance pole.

The TLC083 with a 1-V step response has an 80% overshoot with a natural frequency of 3.5 MHz when configured as a unity gain buffer and with a 10-kΩ feedback resistor. By adding a 10-pF capacitor in parallel with the feedback resistor, the overshoot is reduced to 40% and eliminates the natural frequency, resulting in a much faster settling time (see Figure 49). The 10-pF capacitor was chosen for convenience only.

Load capacitance had little effect on these measurements due to the excellent output drive capability of the TLC08x.
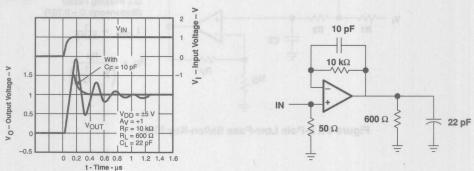
Figure 49. 1-V Step Response

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 50).

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 50. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 51. 2-Pole Low-Pass Sallen-Key Filter

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APPLICATION INFORMATION

shutdown function

Three members of the TLC08x family (TLC080/3/5) have a shutdown terminal ($\overline{\text{SHDN}}$) for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 16 nA/channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to V_{DD}− (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 43 and 44. The amplifier is powered with a single 5-V supply and is configured as noninverting with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 37, 38, 39, and 40 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is configured as a voltage follower (A_V = 1). The isolation performance is plotted across frequency using 0.1 V_{PP}, 2.5 V_{PP}, and 5 V_{PP} input signals at ±2.5 V supplies and 0.1 V_{PP}, 8 V_{PP}, and 12 V_{PP} input signals at ±6 V supplies.

circuit layout considerations

To achieve the levels of high performance of the TLC08x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.

- Proper power supply decoupling – Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.

- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

general PowerPAD™ design considerations

The TLC08x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 52(a) and Figure 52(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 52(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

Side View (a)

End View (b)

Thermal Pad

Bottom View (c)

NOTE B. The thermal pad is electrically isolated from all terminals in the package.

Figure 52. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

Thermal Pad Area

Single or Dual

Quad

68 mils x 70 mils) with 5 vias
(Via diameter = 13 mils

78 mils x 94 mils) with 9 vias
(Via diameter = 13 mils)

Figure 53. PowerPAD PCB Etch and Via Pattern

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APPLICATION INFORMATION

general PowerPAD design considerations (continued)

1. Prepare the PCB with a top side etch pattern as shown in Figure 53. There should be etch for the leads as well as etch for the thermal pad.

2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLC08x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.

4. Connect all holes to the internal ground plane.

5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLC08x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the TLC08x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 54 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLC08x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
  θ_{JC} = Thermal coefficient from junction to case
  θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

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APPLICATION INFORMATION

general PowerPAD design considerations (continued)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

NOTE A.   Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 54. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially muti-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 55 are generated using the TLC08x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1:   G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).

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```
*DEVICE=TLC08X, OPAMP,NPN,INT*DEVICE=TLC08X,
+OPAMP,NPN,INT
* TLC08X operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 07/02/99 at 13:14
* Parts is a MicroSim product.
*
* connections:   non–inverting input
*                 | inverting input
*                 | | positive power supply
*                 | | | negative power supply
*                 | | | | output
*                 | | | | |
.subckt TLC08X    1 2 3 4 5
*
  c1   11 12 4.6015E–12
  c2   6 7 8.0000E–12
  cee  10 99 993.10E–15
  dc   5 53 dy
  de   54 5 dy
  dlp  90 91 dx
  dln  92 90 dx
  dp   4 3 dx
  egnd 99 0 poly(2) (3,0) (4,0) 0 .5 .5
  fb   7 99 poly(5) vb vc ve vlp vln 0 13.984E6 –1E3 1E3
+14E6 –14E6
  ga   6 0 11 12 402.12E–6
  gcm  0 6 10 99 1.5735E–6
```

```
  iee  10 4 dc 130.40E–6
  ioff 0 6 dc 1.235E–6
  hlim 90 0 vlim 1K
  q1   11 2 13 qx1
  q2   12 1 14 qx2
  r2   6 9 100.00E3
  rc1  3 11 2.4868E3
  rc2  3 12 2.4868E3
  re1  13 10 2.0901E3
  re2  14 10 2.0901E3
  ree  10 99 1.5337E6
  ro1  8 5 10
  ro2  7 99 10
  rp   3 4 3.0495E3
  vb   9 0 dc 0
  vc   3 53 dc 1.5537
  ve   54 4 dc .84373
  vlim 7 8 dc 0
  vlp  91 0 dc 117.60
  vln  0 92 dc 117.60
.model dx D(Is=800.00E–18)
.model dy D(Is=800.00E–18 Rs=1m Cjo=10p)
.model qx1 NPN(Is=800.00E–18 Bf=407.50E6)
.model qx2 NPN(Is=800.0000E–18 Bf=407.50E6)
.ends
*$
```

Figure 55. Boyle Macromodel and Subcircuit

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- **Output Swing Includes Both Supply Rails**
- **Extended Common-Mode Input Voltage Range . . . 0 V to 4.5 V (Min) with 5-V Single Supply**
- **No Phase Inversion**
- **Low Noise . . . 18 nV/$\sqrt{Hz}$ Typ at f = 1 kHz**
- **Low Input Offset Voltage 950 µV Max at T_A = 25°C (TLV2422A)**

- **Low Input Bias Current . . . 1 pA Typ**
- **Micropower Operation . . . 50 µA Per Channel**
- **600-Ω Output Drive**
- **Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards**

description

The TLV2422 and TLV2422A are dual low-voltage operational amplifiers from Texas Instruments. The common-mode input voltage range for this device has been extended over the typical CMOS amplifiers making them suitable for a wide range of applications. In addition, the devices do not phase invert when the common-mode input is driven to the supply rails. This satisfies most design requirements without paying a premium for rail-to-rail input performance. They also exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterized at 3-V and 5-V supplies and is optimized for low-voltage operation. The TLV2422 only requires 50 µA of supply current per channel, making it ideal for battery-powered applications. The TLV2422 also has increased output drive over previous rail-to-rail operational amplifiers and can drive 600-Ω loads for telecom applications.

Other members in the TLV2422 family are the high-power, TLV2442, and low-power, TLV2432, versions.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 1

The TLV2422, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels and low-voltage operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV2422A is available with a maximum input offset voltage of 950 µV.

If the design requires single operational amplifiers, see the TI TLV2211/21/31. This is a family of rail-to-rail output operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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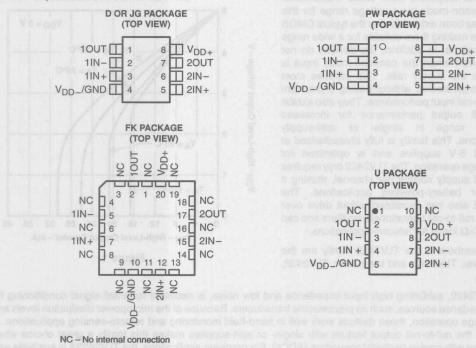
TLV2422, TLV2422A, TLV2422Y
Advanced LinCMOS™ RAIL-TO-RAIL OUTPUT
WIDE-INPUT-VOLTAGE MICROPOWER DUAL OPERATIONAL AMPLIFIERS
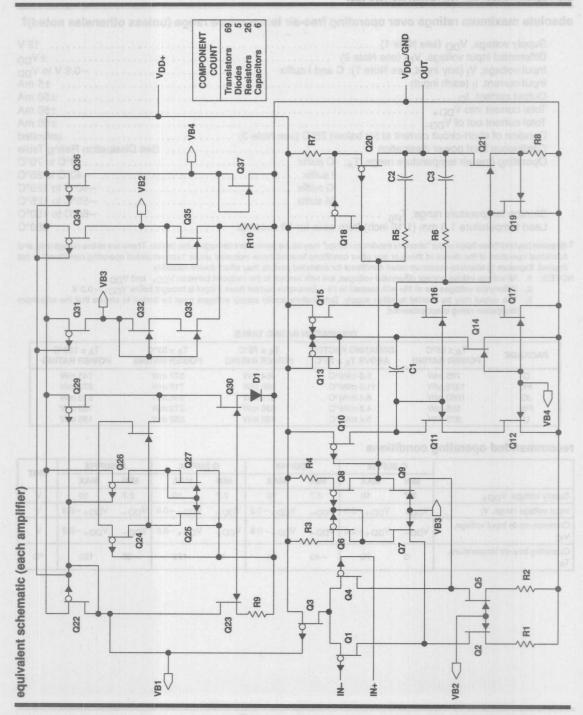
SLOS199B – SEPTEMBER 1997 – REVISED SEPTEMBER 1999

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	TSSOP (PW)	CERAMIC FLAT PACK (U)	
0°C to 70°C	2.5 mV	TLV2422CD	—	—	TLV2422CPWLE	—	
−40°C to 85°C	950 µV	TLV2422AID	—	—	TLV2422AIPWLE	—	
	2.5 mV	TLV2421ID	—	—	—	—	
−40°C to 125°C	950 µV	TLV2422AQD	—	—	—	—	TLV2422Y
	2.5 mV	TLV2422QD	—	—	—	—	
−55°C to 125°C	950 µV	—	TLV2422AMFK	TLV2422AMJG	—	TLV2422AMU	
	2 mV	—	TLV2422MFK	TLV2422MJG	—	TLV2422MU	

The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2422CDR). The PW package is available only left-end taped and reeled. Chips are tested at 25°C.

D OR JG PACKAGE
(TOP VIEW)

1OUT	1	8 $V_{DD}+$
1IN−	2	7 2OUT
1IN+	3	6 2IN−
$V_{DD}-$/GND	4	5 2IN+

PW PACKAGE
(TOP VIEW)

1OUT	1	8 $V_{DD}+$
1IN−	2	7 2OUT
1IN+	3	6 2IN−
$V_{DD}-$/GND	4	5 2IN+

FK PACKAGE
(TOP VIEW)

NC 1OUT NC $V_{DD}+$ NC
3 2 1 20 19

NC	4		18	NC
1IN−	5		17	2OUT
NC	6		16	NC
1IN+	7		15	2IN−
NC	8		14	NC

9 10 11 12 13
NC $V_{DD}-$/GND NC 2IN+ NC

U PACKAGE
(TOP VIEW)

NC	1	10 NC
1OUT	2	9 $V_{DD}+$
1IN−	3	8 2OUT
1IN+	4	7 2IN−
$V_{DD}-$/GND	5	6 2IN+

NC – No internal connection

TEXAS INSTRUMENTS

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equivalent schematic (each amplifier)

COMPONENT COUNT	
Transistors	69
Diodes	5
Resistors	26
Capacitors	6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 12 V
Differential input voltage, V_{ID} (see Note 2) . . . . $\pm V_{DD}$
Input voltage, V_I (any input, see Note 1): C and I suffix . . . . −0.3 V to V_{DD}
Input current, I_I (each input) . . . . $\pm$5 mA
Output current, I_O . . . . $\pm$50 mA
Total current into V_{DD+} . . . . $\pm$50 mA
Total current out of V_{DD-} . . . . $\pm$50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) . . . . unlimited
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
I suffix . . . . −40°C to 85°C
Q suffix . . . . −40°C to 125°C
M suffix . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
2. Differential voltages are at IN+ with respect to IN−. Excessive current flows if input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum
dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$	2.7	10	2.7	10	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V_{DD-}	$V_{DD+}-0.8$	V
Operating free-air temperature, T_A	0	70	−40	85	−40	125	−55	125	°C

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electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422C MIN	TLV2422C TYP	TLV2422C MAX	UNIT
V_{IO}	Input offset voltage			25°C		300	2000	μV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{IC} = 0$, $V_O = 0$,	$V_{DD}\pm = \pm 2.5$ V, $R_S = 50\ \Omega$	25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq 5$ mV,	$R_S = 50\ \Omega$	25°C	0 to 2.5	−0.25 to 2.75		V
				Full range	0 to 2.2			
V_{OH}	High-level output voltage	$I_{OH} = -100\ \mu A$		25°C		2.97		V
		$I_{OH} = -500\ \mu A$		25°C		2.75		
				Full range	2.5			
V_{OL}	Low-level output voltage	$V_{IC} = 0$,	$I_{OL} = 100\ \mu A$	25°C		0.05		V
		$V_{IC} = 0$,	$I_{OL} = 250\ \mu A$	25°C		0.2		
				Full range			0.5	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 2 V	$R_L = 10\ k\Omega$‡	25°C	6	10		V/mV
				Full range	3			
			$R_L = 1\ M\Omega$‡	25°C		700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz		25°C		8		pF
z_O	Closed-loop output impedance	$f = 100$ kHz,	$A_V = 10$	25°C		130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.5 V, $V_O = 1.5$ V, $R_S = 50\ \Omega$		25°C	70	83		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7$ V to 8 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	$V_O = 1.5$ V,	No load	25°C		100	150	μA
				Full range			175	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A[†]	TLV2422I			TLV2422AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		300	2000		300	950	μV
				Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{IC} = 0$, $V_O = 0$,	$V_{DD}\pm = \pm2.5$ V, $R_S = 50\ \Omega$	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le 5$ mV,	$R_S = 50\ \Omega$	25°C	0 to 2.5	−0.25 to 2.75		0 to 2.5	−0.25 to 2.75		V
				Full range	0 to 2.2			0 to 2.2			
V_{OH}	High-level output voltage	$I_{OH} = -100\ \mu A$		25°C		2.97			2.97		V
		$I_{OH} = -500\ \mu A$		25°C		2.75			2.75		
				Full range	2.5			2.5			
V_{OL}	Low-level output voltage	$V_{IC} = 0$,	$I_{OL} = 100\ \mu A$	25°C		0.05			0.05		V
				25°C		0.2			0.2		
		$V_{IC} = 0$,	$I_{OL} = 250\ \mu A$	Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 2 V	$R_L = 10\ k\Omega$[‡]	25°C	6	10		6	10		V/mV
				Full range	3			3			
			$R_L = 1\ M\Omega$[‡]	25°C		700			700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz		25°C		8			8		pF
z_o	Closed-loop output impedance	$f = 100$ kHz,	$A_V = 10$	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.5 V, $R_S = 50\ \Omega$	$V_O = 1.5$ V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$	$V_{DD} = 2.7$ V to 8 V, $V_{IC} = V_{DD}/2$,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	$V_O = 1.5$ V,	No load	25°C		100	150		100	150	μA
				Full range			175			175	

[†] Full range is – 40°C to 85°C.
[‡] Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, V$_{DD}$ = 3 V

PARAMETER		TEST CONDITIONS		T$_A$†	TLV2422C, TLV2422I TLV2422AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V$_O$ = 1.5 V to 3.5 V, C$_L$ = 100 pF‡	R$_L$ = 10 kΩ‡,	25°C	0.01	0.02		V/µs
				Full range	0.008			
V$_n$	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		23		
V$_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		µV
		f = 0.1 Hz to 10 Hz		25°C		4		
I$_n$	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V$_O$ = 0.5 V to 2.5 V, f = 1 kHz, R$_L$ = 10 kΩ‡	A$_V$ = 1	25°C		0.25%		
			A$_V$ = 10			1.8%		
	Gain-bandwidth product	f = 10 kHz, C$_L$ = 100 pF‡	R$_L$ = 10 kΩ‡,	25°C		46		kHz
B$_{OM}$	Maximum output-swing bandwidth	V$_{O(PP)}$ = 1 V, R$_L$ = 10 kΩ‡,	A$_V$ = 1, C$_L$ = 100 pF‡	25°C		8.3		kHz
t$_s$	Settling time	A$_V$ = −1, Step = 0.5 V to 2.5 V, R$_L$ = 10 kΩ‡, C$_L$ = 100 pF‡	To 0.1%	25°C		8.6		µs
			To 0.01%			16		
φ$_m$	Phase margin at unity gain	R$_L$ = 10 kΩ‡,	C$_L$ = 100 pF‡	25°C		62°		
	Gain margin			25°C		11		dB

† Full range for the C version is 0°C to 70°C. Full range for the I version is −40°C to 85°C.
‡ Referenced to 2.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422Q, TLV2422M			TLV2422AQ, TLV2422AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		300	2000		300	950	μV
				Full range			2500			1800	
α_{VIO}	Temperature coefficient of input offset voltage			Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	V_{IC} = 0, V_O = 0,	$V_{DD}\pm$ = ±1.5 V, R_S = 50 Ω	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			300			300	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq 5$ mV,	R_S = 50 Ω	25°C	0 to 2.5	−0.25 to 2.75		0 to 2.5	−0.25 to 2.75		V
				Full range	0 to 2.2			0 to 2.2			
V_{OH}	High-level output voltage	I_{OH} = −100 μA		25°C		2.97			2.97		V
		I_{OH} = −500 μA		25°C		2.75			2.75		
				Full range	2.5			2.5			
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 100 μA	25°C		0.05			0.05		V
				25°C		0.2			0.2		
		V_{IC} = 0,	I_{OL} = 250 μA	Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 10 kΩ‡	25°C	6	10		6	10		V/mV
				Full range	2			2			
			R_L = 1 MΩ‡	25°C		700			700		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8			8		pF
z_O	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ min, V_O = 1.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, $V_{IC} = V_{DD}/2$, No load		25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		100	150		100	150	μA
				Full range			175			175	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2422Q, TLV2422M, TLV2422AQ, TLV2422AM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C	0.01	0.02		V/µs
				Full range	0.008			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		23		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		2.7		µV
		f = 0.1 Hz to 10 Hz		25°C		4		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 1 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.25%		
			A_V = 10			1.8%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		46		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		8.3		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		8.6		µs
			To 0.01%			16		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		62°		
	Gain margin			25°C		11		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2422C			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		300	2000	μV
				Full range			2500	
α_{VIO}	Temperature coefficient of input offset voltage	V_{IC} = 0, $V_{DD}\pm$ = ±2.5 V, V_O = 0, R_S = 50 Ω		25°C to 70°C		2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5		pA
				Full range			150	
I_{IB}	Input bias current			25°C		1		pA
				Full range			150	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq$ 5 mV, R_S = 50 Ω		25°C	0 to 4.5	−0.25 to 4.75		V
				Full range	0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = −100 μA		25°C		4.97		V
		I_{OH} = −1 mA		25°C	4.5	4.75		
				Full range	4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 μA		25°C		0.04		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA		25°C		0.15		
				Full range			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	8	12		V/mV
				Full range	5			
			R_L = 1 MΩ‡	25°C		1000		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_O	Closed-loop output impedance	f = 100 kHz, A_V = 10		25°C		130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	90		dB
				Full range	70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load		25°C	80	95		dB
				Full range	80			
I_{DD}	Supply current	V_O = 2.5 V, No load		25°C		100	150	μA
				Full range			175	

† Full range is 0°C to 70°C.
‡ Referenced to 2.5 V
NOTE 4:   Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2422I MIN	TLV2422I TYP	TLV2422I MAX	TLV2422AI MIN	TLV2422AI TYP	TLV2422AI MAX	UNIT
V_{IO}	Input offset voltage		25°C		300	2000		300	950	μV
			Full range			2500			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	V_{IC} = 0, V_O = 0, $V_{DD}\pm = \pm 2.5$ V, R_S = 50 Ω	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le 5$ mV, R_S = 50 Ω	25°C	0 to 4.5	–0.25 to 4.75		0 to 4.5	–0.25 to 4.75		V
			Full range	0 to 4.2			0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = –100 μA	25°C		4.97			4.97		V
		I_{OH} = –1 mA	25°C	4.5	4.75		4.5	4.75		
			Full range	4.25			4.25			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 μA	25°C		0.04			0.04		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.15			0.15		
			Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ‡	25°C	8	12		8	12		V/mV
			Full range	5			5			
		R_L = 1 MΩ‡	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz	25°C		8			8		pF
z_O	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 4.5 V, V_O = 2.5 V, R_S = 50 Ω	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		100	150		100	150	μA
			Full range			175			175	

† Full range is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V

	PARAMETER	TEST CONDITIONS		T_A†	TLV2422C, TLV2422I TLV2422AI			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 10 kΩ‡	25°C	0.01	0.02		V/µs
				Full range	0.008			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		µV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	V_O = 1.5 V to 3.5 V, f = 1 kHz, R_L = 10 kΩ‡	A_V = 1	25°C		0.24%		
			A_V = 10			1.7%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L =10 kΩ‡,	25°C		52		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		5.3		kHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 10 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		8.5		µs
			To 0.01%			15.5		
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		66°		
	Gain margin			25°C		11		dB

† Full range for the C version is 0°C to 70°C. Full range for the I version is –40°C to 85°C.
‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2422Q, TLV2422M			TLV2422AQ, TLV2422AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		300	2000		300	950	μV
			Full range			2500			1800	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)	V_{IC} = 0, V_O = 0,	$V_{DD}±$ = ±2.5 V, R_S = 50 Ω	25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			300			300	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq 5$ mV, R_S = 50 Ω		25°C	0 to 4.5	−0.25 to 4.75		0 to 4.5	−0.25 to 4.75		V
				Full range	0 to 4.2			0 to 4.2			
V_{OH}	High-level output voltage	I_{OH} = −100 μA	25°C		4.97			4.97		V
		I_{OH} = −1 mA	25°C		4.75			4.75		
			Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 100 μA	25°C		0.04			0.04		V
		V_{IC} = 2.5 V, I_{OL} = 500 μA	25°C		0.15			0.15		
			Full range			0.5			0.5	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ‡	25°C	8	12		8	12		V/mV
			Full range	3			3			
		R_L = 1 MΩ‡	25°C		1000			1000		
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz	25°C		8			8		pF
z_O	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		130			130		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min, V_O = 2.5 V, R_S = 50 Ω	25°C	70	90		70	90		dB
			Full range	70			70			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2, No load	25°C	80	95		80	95		dB
			Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		100	150		100	150	μA
			Full range			175			175	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD} = 5$ V

	PARAMETER	TEST CONDITIONS		T_A†	TLV2422Q, TLV2422M, TLV2422AQ, TLV2422AM			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5$ V to 3.5 V, $C_L = 100$ pF‡	$R_L = 10$ kΩ‡,	25°C	0.01	0.02		V/µs
				Full range	0.008			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100		nV/√Hz
		f = 1 kHz		25°C		18		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.9		µV
		f = 0.1 Hz to 10 Hz		25°C		2.8		
I_n	Equivalent input noise current			25°C		0.6		fA√Hz
THD + N	Total harmonic distortion plus noise	$V_O = 1.5$ V to 3.5 V, f = 1 kHz, $R_L = 10$ kΩ‡	$A_V = 1$	25°C		0.24%		
			$A_V = 10$			1.7%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF‡	$R_L = 10$ kΩ‡,	25°C		52		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2$ V, $R_L = 10$ kΩ‡,	$A_V = 1$, $C_L = 100$ pF‡	25°C		5.3		kHz
t_s	Settling time	$A_V = -1$, Step = 1.5 V to 3.5 V, $R_L = 10$ kΩ‡, $C_L = 100$ pF‡	To 0.1%	25°C		8.5		µs
			To 0.01%			15.5		
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ‡,	$C_L = 100$ pF‡	25°C		66°		
	Gain margin			25°C		11		dB

† Full range is –40°C to 125°C for Q level part, –55°C to 125°C for M level part.
‡ Referenced to 2.5 V

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TYPICAL CHARACTERISTICS

Table of Graphs

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		vs Common-mode input voltage	4,5
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V_{OH}	High-level output voltage	vs High-level output current	9,11
V_{OL}	Low-level output voltage	vs Low-level output current	10,12
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	13
I_{OS}	Short-circuit output current	vs Supply voltage	14
		vs Free-air temperature	15
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	Differential gain	vs Load resistance	18
A_{VD}	Large-signal differential voltage amplification	vs Frequency	19,20
		vs Free-air temperature	21,22
z_o	Output impedance	vs Frequency	23,24
CMRR	Common-mode rejection ratio	vs Frequency	25
		vs Free-air temperature	26
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	27,28
		vs Free-air temperature	29
I_{DD}	Supply current	vs Supply voltage	30
SR	Slew rate	vs Load capacitance	31
		vs Free-air temperature	32
V_O	Inverting large-signal pulse response		33,34
V_O	Voltage-follower large-signal pulse response		35,36
V_O	Inverting small-signal pulse response		37,38
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ϕ_m	Phase margin	vs Frequency	19,20
		vs Load capacitance	48
	Gain margin	vs Load capacitance	49
B_1	Unity-gain bandwidth	vs Load capacitance	50

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE

452 Amplifiers from 1 Wafer Lot
V_{DD} = 3 V
R_L = 10 kΩ
T_A = 25°C

V_{IO} – Input Offset Voltage – mV

Figure 2

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE

454 Amplifiers from 1 Wafer Lot
V_{DD} = 5 V
R_L = 10 kΩ
T_A = 25°C

V_{IO} – Input Offset Voltage – mV

Figure 3

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

V_{DD} = 3 V

V_{IC} – Common-Mode Input Voltage – V

Figure 4

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

V_{DD} = 5 V

V_{IC} – Common-Mode Input Voltage – V

Figure 5

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

32 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 1.5$ V
$T_A = 25°C$ to $125°C$

Figure 6

DISTRIBUTION OF TLV2422 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

32 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 2.5$ V
$T_A = 25°C$ to $125°C$

Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

$V_{DD} = \pm 2.5$ V

Figure 8

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

$V_{DD} = 3$ V

Figure 9

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

V_{DD} = 3 V

T_A = 125°C

T_A = 85°C

T_A = 25°C

T_A = –40°C

V_{OL} – Low-Level Output Voltage – V

I_{OL} – Low-Level Output Current – mA

Figure 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

V_{DD} = 5 V

T_A = –40°C

T_A = 25°C

T_A = 85°C

T_A = 125°C

V_{OH} – High-Level Output Voltage – V

I_{OH} – High-Level Output Current – mA

Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

V_{DD} = 5 V

T_A = 125°C

T_A = 85°C

T_A = 25°C

T_A = –40°C

V_{OH} – High-Level Output Voltage – V

I_{OL} – Low-Level Output Current – mA

Figure 12

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

V_{DD} = 5 V

R_L = 10 kΩ
T_A = 25°C

V_{DD} = 3 V

$V_{O(PP)}$ – Maximum Peak-to-Peak Output Voltage – V

f – Frequency – Hz

Figure 13

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TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 14

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

Figure 15

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

Figure 16

DIFFERENTIAL INPUT VOLTAGE
vs
OUTPUT VOLTAGE

Figure 17

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TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN
vs
LOAD RESISTANCE

Figure 18

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

Figure 19

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 21

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 22

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 23

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 24

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 25

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

Figure 26

TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 27

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 28

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

Figure 29

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 30

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TYPICAL CHARACTERISTICS

SLEW RATE
vs
LOAD CAPACITANCE

Figure 31

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 32

INVERTING LARGE SIGNAL
PULSE RESPONSE

Figure 33

INVERTING LARGE SIGNAL
PULSE RESPONSE

Figure 34

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TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE SIGNAL PULSE RESPONSE

$V_{DD} = 3$ V
$R_L = 10$ kΩ
$C_L = 100$ pF
$A_V = 1$
$T_A = 25°C$

Figure 35

VOLTAGE-FOLLOWER LARGE SIGNAL PULSE RESPONSE

$V_{DD} = 5$ V
$R_L = 10$ kΩ
$C_L = 100$ pF
$A_V = 1$
$T_A = 25°C$

Figure 36

INVERTING SMALL SIGNAL PULSE RESPONSE

$V_{DD} = 3$ V
$R_L = 10$ kΩ
$C_L = 100$ pF
$A_V = -1$
$T_A = 25°C$

Figure 37

INVERTING SMALL SIGNAL PULSE RESPONSE

$V_{DD} = 5$ V
$R_L = 10$ kΩ
$C_L = 100$ pF
$A_V = -1$
$T_A = 25°C$

Figure 38

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

V_{DD} = 3 V
R_L = 10 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

Figure 39

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE

V_{DD} = 5 V
R_L = 10 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

Figure 40

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

V_{DD} = 3 V
T_A = 25°C
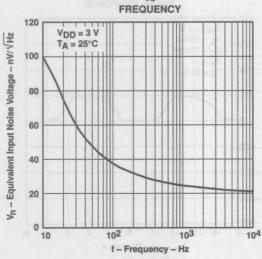
Figure 41

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY
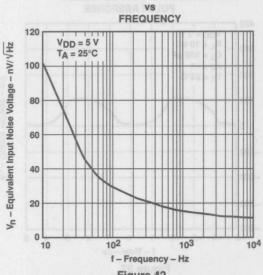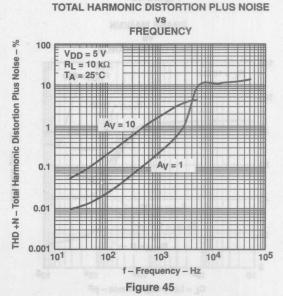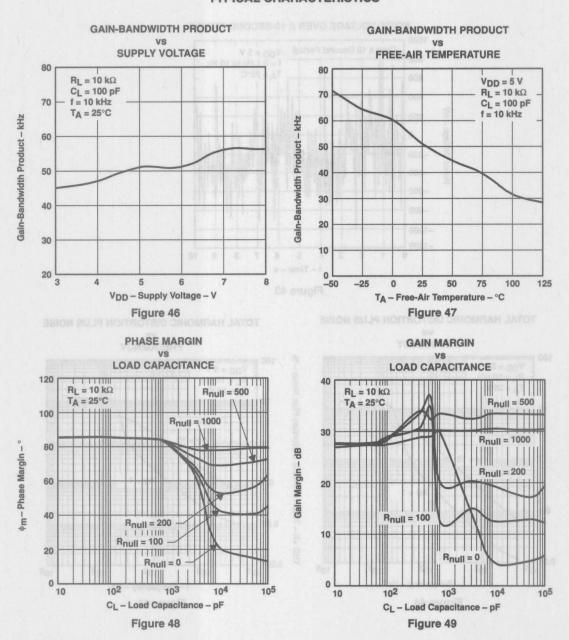
V_{DD} = 5 V
T_A = 25°C

Figure 42

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TYPICAL CHARACTERISTICS

NOISE VOLTAGE OVER A 10-SECOND PERIOD

Over a 10 Second Period $V_{DD} = 5\ V$
$f = 0.1\ Hz\ to\ 10\ Hz$
$T_A = 25°C$

Noise Voltage – nV

t – Time – s

Figure 43

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

THD +N – Total Harmonic Distortion Plus Noise – %

$V_{DD} = 3\ V$
$R_L = 10\ k\Omega$
$T_A = 25°C$

$A_V = 10$

$A_V = 1$

f – Frequency – Hz

Figure 44

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

THD +N – Total Harmonic Distortion Plus Noise – %

$V_{DD} = 5\ V$
$R_L = 10\ k\Omega$
$T_A = 25°C$

$A_V = 10$

$A_V = 1$

f – Frequency – Hz

Figure 45

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

$R_L = 10\ k\Omega$
$C_L = 100\ pF$
$f = 10\ kHz$
$T_A = 25°C$

Figure 46

GAIN-BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

$V_{DD} = 5\ V$
$R_L = 10\ k\Omega$
$C_L = 100\ pF$
$f = 10\ kHz$

Figure 47

PHASE MARGIN
vs
LOAD CAPACITANCE

$R_L = 10\ k\Omega$
$T_A = 25°C$

$R_{null} = 500$
$R_{null} = 1000$
$R_{null} = 200$
$R_{null} = 100$
$R_{null} = 0$

Figure 48

GAIN MARGIN
vs
LOAD CAPACITANCE

$R_L = 10\ k\Omega$
$T_A = 25°C$

$R_{null} = 500$
$R_{null} = 1000$
$R_{null} = 200$
$R_{null} = 100$
$R_{null} = 0$

Figure 49

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

Figure 50

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

Figure 30

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23-µA 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

- Supply Current . . . 23 µA/Channel
- Gain-Bandwidth Product . . . 220 kHz
- Output Drive Capability . . . ±10 mA
- Input Offset Voltage . . . 20 µV (typ)
- V_{DD} Range . . . 2.7 V to 6 V
- Power Supply Rejection Ratio . . . 106 dB
- Ultra-Low Power Shutdown Mode
  I_{DD} . . . 16 nA/ch
- Rail-To-Rail Input/Output (RRIO)
- Ultra-Small Packaging
  - 5 or 6 Pin SOT-23 (TLV2450/1)
  - 8 or 10 Pin MSOP (TLV2452/3)

TLV2450
DBV† PACKAGE
(TOP VIEW)

OUT	1	6	$V_{DD}+$
GND	2	5	SHDN
IN+	3	4	IN–

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

description

The TLV245x is a family of rail-to-rail input/output operational amplifiers that set a new performance point for supply current and ac performance. These devices consume a mere 23 µA/channel while offering 220 kHz of gain bandwidth product; much higher than competitive devices with similar supply current levels. Along with increased ac performance, the amplifier provides high output drive capability, solving a major shortcoming of older micropower rail-to-rail input/output operational amplifiers. The TLV245x can swing to within 250 mV of each supply rail while driving a 2.5-mA load. Both the inputs and outputs swing rail-to-rail for increased dynamic range in low-voltage applications. This performance makes the TLV245x family ideal for portable medical equipment, patient monitoring systems, and data acquisition circuits.

Three members of the family (TLV2450/3/5) offer a shutdown terminal for conserving battery life in portable applications. During shutdown, the outputs are placed in a high-impedance state and the amplifier consumes only 16 nA/channel. The family is fully specified at 3 V and 5 V across an expanded industrial temperature range (–40°C to 125°C). The singles and duals are available in the SOT23 and MSOP packages, while the quads are available in TSSOP. The TLV2450 offers an amplifier with shutdown functionality all in a 6-pin SOT23 package, making it perfect for high density circuits.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2450	1	8	8	6‡	—	—	Yes	UNIV-OPAMP–2
TLV2451	1	8	8	5	—	—	—	UNIV-OPAMP–1
TLV2452	2	8	8	—	—	8	—	UNIV-OPAMP–1
TLV2453	2	14	14	—	—	10	Yes	UNIV-OPAMP–2
TLV2454	4	14	14	—	14	—	—	—
TLV2455	4	16	16	—	16	—	Yes	—

‡ This device is in the Product Preview stage of development. Contact your local TI sales office for availability.

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TLV2450 and TLV2451 AVAILABLE OPTIONS

T$_A$	PACKAGED DEVICES					CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	SOT-23			PLASTIC DIP (P)	
		(DBV)†	SYMBOL			
0°C to 70°C	TLV2450CD§ TLV2451CD	TLV2450CDBV TLV2451CDBV	VAQC VARC		TLV2450CP TLV2451CP	TLV2450Y TLV2451Y
−40°C to 125°C	TLV2450ID§ TLV2451ID	TLV2450IDBV TLV2451IDBV	VAQI VARI		TLV2450IP TLV2451IP	— —
	TLV2450AID TLV2451AID	— —	— —		TLV2450AIP TLV2451AIP	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2450CDR).
‡ Chip forms are tested at T$_A$ = 25°C only.
§ This device is in the Produact Preview stage of development. Contacat your local TI sales office for availability.

TLV2452 and TLV2453 AVAILABLE OPTIONS

T$_A$	PACKAGED DEVICES							CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)	
		(DGK)†	SYMBOL§	(DGS)†	SYMBOL§			
0°C to 70°C	TLV2452CD TLV2453CD	TLV2452CDGK —	xxTIABI —	— TLV2453CDGS	— xxTIABK	— TLV2453CN	TLV2452CP —	TLV2452Y TLV2453Y
−40°C to 125°C	TLV2452ID TLV2453ID	TLV2452IDGK —	xxTIABJ —	— TLV2453IDGS	— xxTIABL	— TLV2453IN	TLV2452IP —	— —
	TLV2452AID TLV2453AID	— —	— —	— —	— —	— TLV2453AIN	TLV2452AIP —	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2452CDR).
‡ Chip forms are tested at T$_A$ = 25°C only.
§ xx represents the device date code.

TLV2454 and TLV2455 AVAILABLE OPTIONS

T$_A$	PACKAGED DEVICES			CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PW)†	
0°C to 70°C	TLV2454CD TLV2455CD	TLV2454CN TLV2455CN	TLV2454CPW TLV2455CPW	TLV2454Y TLV2455Y
−40°C to 125°C	TLV2454ID TLV2455ID	TLV2454IN TLV2455IN	TLV2454IPW TLV2455IPW	— —
	TLV2454AID TLV2455AID	TLV2454AIN TLV2455AIN	TLV2454AIPW TLV2455AIPW	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2454CDR).
‡ Chip forms are tested at T$_A$ = 25°C only.

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TLV245x PACKAGE PINOUTS

TLV2450
DBV PACKAGE
(TOP VIEW)

OUT 1	6 V$_{DD+}$
GND 2	5 SHDN
IN+ 3	4 IN−

TLV2451
DBV PACKAGE
(TOP VIEW)

OUT 1	5 V$_{DD+}$
GND 2	
IN+ 3	4 IN−

TLV2452
D, DGN, OR P PACKAGE
(TOP VIEW)

1OUT 1	8 V$_{DD+}$
1IN− 2	7 2OUT
1IN+ 3	6 2IN−
GND 4	5 2IN+

TLV2450
D OR P PACKAGE
(TOP VIEW)

NC 1	8 SHDN
IN− 2	7 V$_{DD+}$
IN+ 3	6 OUT
GND 4	5 NC

TLV2451
D OR P PACKAGE
(TOP VIEW)

NC 1	8 NC
IN− 2	7 V$_{DD+}$
IN+ 3	6 OUT
GND 4	5 NC

TLV2453
DGS PACKAGE
(TOP VIEW)

1OUT 1	10 V$_{DD+}$
1IN− 2	9 2OUT
1IN+ 3	8 2IN−
GND 4	7 2IN+
1SHDN 5	6 2SHDN

TLV2453
D OR N PACKAGE
(TOP VIEW)

1OUT 1	14 V$_{DD+}$
1IN− 2	13 2OUT
1IN+ 3	12 2IN−
GND 4	11 2IN+
NC 5	10 NC
1SHDN 6	9 2SHDN
NC 7	8 NC

TLV2454
D, N, OR PW PACKAGE
(TOP VIEW)

1OUT 1	14 4OUT
1IN− 2	13 4IN−
1IN+ 3	12 4IN+
V$_{DD+}$ 4	11 GND
2IN+ 5	10 3IN+
2IN− 6	9 3IN−
2OUT 7	8 3OUT

TLV2455
D, N, OR PW PACKAGE
(TOP VIEW)

1OUT 1	16 4OUT
1IN− 2	15 4IN−
1IN+ 3	14 4IN+
V$_{DD+}$ 4	13 GND
2IN+ 5	12 3IN+
2IN− 6	11 3IN−
2OUT 7	10 3OUT
1/2SHDN 8	9 3/4SHDN

NC − No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 7 V

Differential input voltage, V_{ID} .... $\pm V_{DD}$

Continuous total power dissipation .... See Dissipation Rating Table

Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C

I suffix .... −40°C to 125°C

Maximum junction temperature, T_J .... 150°C

Storage temperature range, T_{stg} .... −65°C to 150°C

Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to V_{DD}−.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGK (8)	54.2	259.9	481 mW
DGS (10)	54.1	257.7	485 mW
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW
PW (16)	28.7	161.4	774 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		V_{DD}−	V_{DD}+	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	−40	125	

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electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV245x			25°C		20	1500	μV
					Full range			2000	
		TLV245xA			25°C		20	1000	
					Full range			1300	
α_{VIO}	Temperature coefficient of input offset voltage		$V_{DD} = \pm1.5$ V, $V_{IC} = 0$,	$V_O = 0$, $R_S = 50\ \Omega$			0.3		μV/°C
I_{IO}	Input offset current				25°C		0.3	4.5	nA
					Full range			5.5	
I_{IB}	Input bias current				25°C		0.9	5	nA
					Full range			7	
V_{ICR}	Common-mode input voltage range		CMRR > 70 dB	$R_S = 50\ \Omega$	25°C	0 to 3			V
			CMRR > 52 dB	$R_S = 50\ \Omega$	Full range	0 to 3			
V_{OH}	High-level output voltage		$V_{IC} = 1.5$ V,	$I_{OH} = -500$ μA	25°C	2.85	2.95		V
					Full range	2.83			
V_{OL}	Low-level output voltage		$V_{IC} = 1.5$ V,	$I_{OL} = 500$ μA	25°C		0.09	0.16	V
					Full range			0.2	
I_{OS}	Short-circuit output current		Sourcing		25°C	4	12		mA
					Full range	3			
			Sinking		25°C	2	7		
					Full range	1			
I_O	Output current		$V_O = 0.5$ V from rail		25°C		±4		mA
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)} = 1$ V,	$R_L = 10$ kΩ	25°C	96	110		dB
					Full range	91			
$r_{i(d)}$	Differential input resistance				25°C		10^9		Ω
C_{IC}	Common-mode input capacitance		$f = 10$ kHz		25°C		4.5		pF
z_O	Closed-loop output impedance		$f = 10$ kHz,	$A_V = 10$	25°C		80		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = 0$ to 3 V, $R_S = 50\ \Omega$	TLV245xC	Full range	60			dB
				TLV245xI		52			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 2.7$ V to 6 V, No load	$V_{IC} = V_{DD}/2$,	25°C	76	89		dB
					Full range	74			
			$V_{DD} = 3$ V to 5 V, No load	$V_{IC} = V_{DD}/2$,	25°C	88	106		
					Full range	84			

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load		25°C		23	35	μA
			TLV245xC	Full range			40	
			TLV245xI	Full range			45	
$V_{(ON)}$	Turnon voltage level	A_V = 1		25°C		1.73		V
$V_{(OFF)}$	Turnoff voltage level	A_V = 1		25°C		1.45		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)	$\overline{SHDN}$ = < 1.45 V		25°C		12	70	nA
			TLV245xC	Full range			70	
			TLV245xI	Full range			80	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	0.05	0.11		V/μs
				Full range	0.02			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		49		nV/√Hz
		f = 1 kHz		25°C		51		
I_n	Equivalent input noise current	f = 1 kHz		25°C		3.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 1.5 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.04%		
			A_V = 10			0.3%		
			A_V = 100			1.5%		
$t_{(on)}$	Amplifier turnon time	A_V = 5, Measured at 50% point	R_L = OPEN,	25°C		59		μs
$t_{(off)}$	Amplifier turnoff time			25°C		836		ns
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		200		kHz
t_S	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		26		μs
			0.01%			31		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			26		
			0.01%			31		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		56°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		7		dB

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

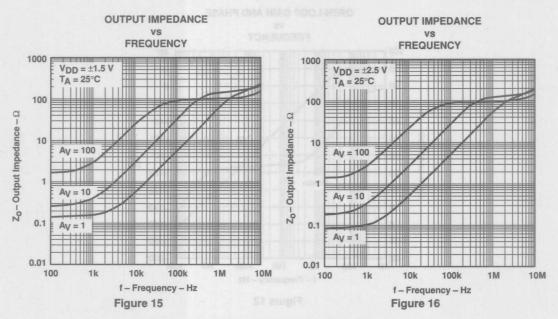| PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV245x			25°C		20	1500	μV
					Full range			2000	
		TLV245xA			25°C		20	1000	
					Full range			1300	
$α_{VIO}$	Temperature coefficient of input offset voltage		V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω			0.3		μV/°C
I_{IO}	Input offset current				25°C		0.3	4.5	nA
					Full range			5.5	
I_{IB}	Input bias current				25°C		0.5	5	nA
					Full range			7	
V_{ICR}	Common-mode input voltage range		CMRR > 70 dB	R_S = 50 Ω	25°C	0 to 5			V
			CMRR > 52 dB	R_S = 50 Ω	Full range	0 to 5			
V_{OH}	High-level output voltage		V_{IC} = 2.5 V,	I_{OH} = −500 μA	25°C	4.87	4.97		V
					Full range	4.85			
V_{OL}	Low-level output voltage		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.07	0.15	V
					Full range			0.16	
I_{OS}	Short-circuit output current		Sourcing		25°C	20	32		mA
					Full range	18			
			Sinking		25°C	12	18		
					Full range	10			
I_O	Output current		V_O = 0.5 V from rail		25°C		±10		mA
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)}$ = 3 V,	R_L = 10 kΩ	25°C	96	103		dB
					Full range	91			
$r_{i(d)}$	Differential input resistance				25°C		10^9		Ω
C_{IC}	Common-mode input capacitance		f = 10 kHz		25°C		4.5		pF
z_o	Closed-loop output impedance		f = 10 kHz,	A_V = 10	25°C		45		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 5 V, R_S = 50 Ω	TLV245xC	Full range	66			dB
				TLV245xI		52			
k_{SVR}	Supply voltage rejection ratio ($ΔV_{DD}$ /$ΔV_{IO}$)		V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	76	89		dB
					Full range	74			
			V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	88	106		
					Full range	84			

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load		25°C		23	42	µA
			TLV245xC	Full range			44	
			TLV245xI	Full range			46	
$V_{(ON)}$	Turnon voltage level	A_V = 1		25°C		1.73		V
$V_{(OFF)}$	Turnoff voltage level	A_V = 1		25°C		1.45		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)	$\overline{SHDN}$ = < 1.45 V		25°C		16	65	nA
			TLV245xC	Full range			65	
			TLV245xI	Full range			80	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	0.05	0.11		V/µs
				Full range	0.02			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		49		nV/√Hz
		f = 1 kHz		25°C		52		
I_n	Equivalent input noise current	f = 1 kHz		25°C		3.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.18%		
			A_V = 100			0.9%		
$t_{(on)}$	Amplifier turnon time	A_V = 5,	R_L = OPEN,	25°C		59		µs
$t_{(off)}$	Amplifier turnoff time	Measured at 50% point		25°C		836		ns
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		220		kHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		24		µs
			0.01%			30		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			25		
			0.01%			30		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		56°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		7		dB

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

TYPICAL CHARACTERISTICS

Table of Graphs
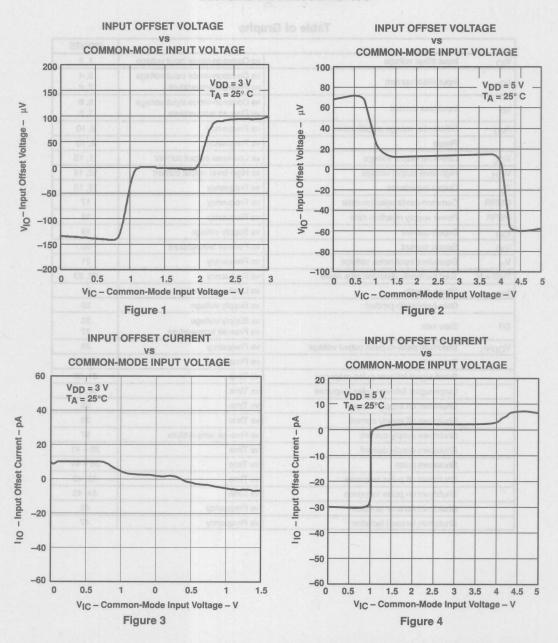
			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IO}	Input offset current	vs Common-mode input voltage	3, 4
		vs Free-air temperature	7, 8
I_{IB}	Input bias current	vs Common-mode input voltage	5, 6
		vs Free-air temperature	7, 8
A_{VD}	Differential voltage amplification	vs Frequency	9, 10
	Phase	vs Frequency	9, 10
V_{OL}	Low-level output voltage	vs Low-level output current	11, 13
V_{OH}	High-level output voltage	vs High-level output current	12, 14
Z_O	Output impedance	vs Frequency	15, 16
CMRR	Common-mode rejection ratio	vs Frequency	17
PSRR	Power supply rejection ratio	vs Frequency	18
I_{DD}	Supply current	vs Supply voltage	19
I_{DD}	Supply current	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD + N	Total harmonic distortion plus noise	vs Frequency	22, 23
ϕ_m	Phase margin	vs Load capacitance	24
	Gain-bandwidth product	vs Supply voltage	25
SR	Slew rate	vs Supply voltage	26
		vs Free-air temperature	27
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	28
	Crosstalk	vs Frequency	29, 30
	Small-signal follower pulse response	vs Time	31, 33
	Large-signal follower pulse response	vs Time	32, 34
	Shutdown on supply current	vs Time	35
	Shutdown off supply current	vs Time	36
	Shutdown supply current	vs Free-air temperature	37
	Shutdown supply current	vs Time	38 – 41
	Shutdown pulse	vs Time	38 – 41
	Shutdown off pulse response	vs Time	42, 43
	Shutdown on pulse response	vs Time	44, 45
	Shutdown reverse isolation	vs Frequency	46
	Shutdown forward isolation	vs Frequency	47

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

Figure 2

INPUT OFFSET CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 3

INPUT OFFSET CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 4

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TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 5

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 6

INPUT OFFSET CURRENT
AND INPUT BIAS CURRENT
vs
FREE–AIR TEMPERATURE

Figure 7

INPUT OFFSET CURRENT
AND INPUT BIAS CURRENT
vs
FREE–AIR TEMPERATURE

Figure 8

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE
vs
FREQUENCY

$V_{DD} = \pm 1.5$ V
$T_A = 25°C$

Gain

Phase

Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE
vs
FREQUENCY

$V_{DD} = \pm 2.5$ V_{DC}
$T_A = 25°C$

Gain

Phase

Figure 10

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 11

Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 13

Figure 14

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 15

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 16

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 17

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

Figure 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 20

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

Figure 21

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

$V_{DD} = 3$ V
$V_{O(PP)} = 1.5$ V
$R_L = 10$ kΩ
$T_A = 25°$ C

$A_V = 10$
$A_V = 100$
$A_V = 1$

f – Frequency – MHz

Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

$V_{DD} = 5$ V
$V_{O(PP)} = 3$ V
$R_L = 10$ kΩ
$T_A = 25°$ C

$A_V = 100$
$A_V = 10$
$A_V = 1$

f – Frequency – Hz

Figure 23

PHASE MARGIN
vs
LOAD CAPACITANCE

$R_{NULL} = 500Ω$
$R_{NULL} = 200Ω$
$R_{NULL} = 100Ω$
$R_{NULL} = 50Ω$
$R_{NULL} = 10Ω$
$R_{NULL} = 0Ω$

$V_{DD} = 5$ V
$R_L = 10$ kΩ
$T_A = 25°$ C

ϕ m – Phase Margin

C_L – Load Capacitance – pF

Figure 24

GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

f = 1 kHz
$R_L = 10$ kΩ
$T_A = 25°$ C

Gain-Bandwidth Product – kHz

V_{DD} – Supply Voltage – V

Figure 25

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TYPICAL CHARACTERISTICS

SLEW RATE
vs
SUPPLY VOLTAGE

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 26

Figure 27

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 28

TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA
FAMILY OF 23-μA 220-kHz RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218B – DECEMBER 1998 – REVISED JUNE 1999
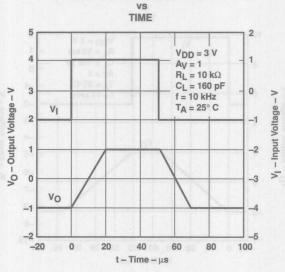
TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

V_{DD} = 3 V
A_V = 1
R_L = 10 kΩ
All Channels

Figure 29

CROSSTALK
vs
FREQUENCY

V_{DD} = 5 V
A_V = 1
R_L = 10 kΩ
All Channels

Figure 30

SMALL-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

V_I

V_O

V_{DD} = 3 V
R_L = 10 kΩ
C_L = 160 pF
A_V = 1
T_A = 25°C
f = 45 kHz

Figure 31

TYPICAL CHARACTERISTICS

LARGE-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

$V_{DD} = 3\ V$
$A_V = 1$
$R_L = 10\ k\Omega$
$C_L = 160\ pF$
$f = 10\ kHz$
$T_A = 25°\ C$

Figure 32

SMALL-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

$V_{DD} = 5\ V$
$A_V = 1$
$R_L = 10\ k\Omega$
$C_L = 160\ pF$
$T_A = 25°\ C$

Figure 33

![Texas Instruments logo]

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

V_{DD} = 5 V
R_L = 10 kΩ
C_L = 160 pF
A_V = 1
T_A = 25°C
f = 10 kHz
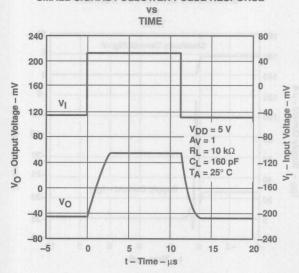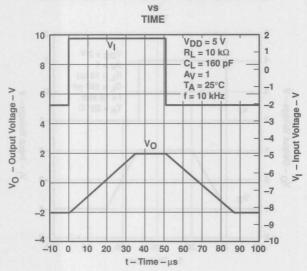
Figure 34

SHUTDOWN ON SUPPLY CURRENT
vs
TIME
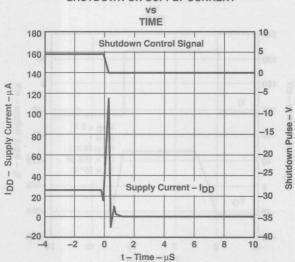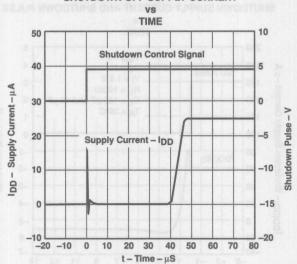
Figure 35

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TYPICAL CHARACTERISTICS

SHUTDOWN OFF SUPPLY CURRENT
vs
TIME

Figure 36

SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 37

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME

V_{DD} = 3 V
A_V = 1
V_I = 1.5 V
R_L = 10 kΩ
C_L = 160 pF and 10 pF
T_A = 25°C

SD Pulse

$I_{DD(SD)}$

t – Time – μs
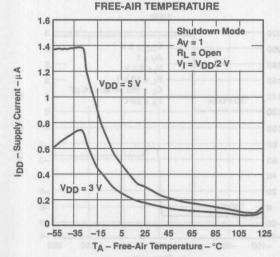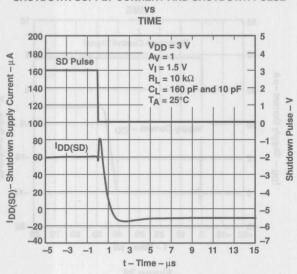
Figure 38

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME

V_{DD} = 5 V
A_V = 1
V_I = 2.5 V
R_L = 10 kΩ
C_L = 160 pF and 10 pF
T_A = 25°C

SD Pulse

$I_{DD(SD)}$

t – Time – μs

Figure 39

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TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME

$V_{DD} = 3$ V
$A_V = 1$
$V_I = 1.5$ V
$R_L = 10$ kΩ
$C_L = 160$ pF and 10 pF
$T_A = 25°C$

Figure 40

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME

$V_{DD} = 5$ V
$A_V = 1$
$V_I = 2.5$ V
$R_L = 10$ kΩ
$C_L = 160$ pF and 10 pF
$T_A = 25°C$

Figure 41

TYPICAL CHARACTERISTICS

SHUTDOWN OFF PULSE RESPONSE
vs
TIME

V_{DD} = 3 V
A_V = 1
V_I = 2.5 V
R_L = 10 kΩ
C_L = 160 pF and 8 pF
T_A = 25°C

SD Pulse

V_O Channel 1

Figure 42

SHUTDOWN OFF PULSE RESPONSE
vs
TIME

SD Pulse

V_O Channel 1

V_{DD} = 5 V
A_V = 1
V_I = 4 V
R_L = 10 kΩ
C_L = 160 pF and 8 pF
T_A = 25°C

Figure 43

SHUTDOWN ON PULSE RESPONSE
vs
TIME

V_{DD} = 3 V
A_V = 1
V_I = 2.5 V
R_L = 10 kΩ
T_A = 25°C

SD Pulse

C_L = 160 pF

C_L = 8 pF

Figure 44

SHUTDOWN ON PULSE RESPONSE
vs
TIME

V_{DD} = 5 V
A_V = 1
V_I = 4 V
R_L = 10 kΩ
T_A = 25°C

SD Pulse

C_L = 160 pF

C_L = 8 pF

Figure 45

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TYPICAL CHARACTERISTICS

SHUTDOWN REVERSE ISOLATION
vs
FREQUENCY

V_{DD} = 3 V and 5 V
$V_{I(PP)}$ = 0.1, 1.5, 2.5 V
R_L = 10 kΩ
C_L = 28 pF
T_A = 25°C

Shutdown Reverse Isolation – dB

f – Frequency – Hz

Figure 46

SHUTDOWN FORWARD ISOLATION
vs
FREQUENCY

V_{DD} = 3 V and 5 V
$V_{I(PP)}$ = 0.1, 1.5, 2.5 V
R_L = 10 kΩ
C_L = 28 pF
T_A = 25°C

Shutdown Forward Isolation – dB

f – Frequency – Hz

Figure 47

APPLICATION INFORMATION

general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 48 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX}-T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV245x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
  θ_{JC} = Thermal coefficient from junction to case
  θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

NOTE A.   Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 48. Maximum Power Dissipation vs Free-Air Temperature

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APPLICATION INFORMATION

shutdown function

Three members of the TLV245x family (TLV2450/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 16 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 42, 43, 44, and 45. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 46 and 47 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35-V supplies and configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency using 0.1-V_{PP}, 1.5-V_{PP}, and 2.5-V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.5-V_{PP} input signal with a supply voltage of ±1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 49 are generated using the TLV245x typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION


```
* AMP_TLV2450-X operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 10/12/98 at 11:06
* Parts is a MicroSim product.
*
* connections:   non–inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt AMP_TLV2450-X 1 2 3 4 5
         c1     11    12    354.48E-15
         c2      6     7    7.5000E-12
         cee    10    99    42.237E-15
         dc      5    53    dy
         de     54     5    dy
         dlp    90    91    dx
         dln    92    90    dx
         dp      4     3    dx
         egnd   99     0    poly(2) (3,0) (4,0) 0 .5 .5
         fb      7    99    poly(5) vb vc ve vlp vln 0
       + 207.31E6 –1E3 1E3 210E6 –210E6
         ga      6     0    11   12 15.254E-6
         gcm     0     6    10   99 48.237E-12

         iee    10     4    dc    938.61E-9
         hlim   90     0    vlim 1K
         q1     11     2    13 qx1
         q2     12     1    14 qx2
         r2      6     9    100.00E3
         rc1     3    11    65.557E3
         rc2     3    12    65.557E3
         re1    13    10    10.367E3
         re2    14    10    10.367E3
         ree    10    99    213.08E6
         ro1     8     5    10
         ro2     7    99    10
         rp      3     4    147.06
         vb      9     0    dc 0
         vc      3    53    dc .82
         ve     54     4    dc .82
         vlim    7     8    dc 0
         vlp    91     0    dc 38
         vln     0    92    dc 38
         .model  dx   D(Is=800.00E-18)
         .model  dy   D(Is=800.00E-18 Rs=1m Cjo=10p)
         .model  qx1  NPN(Is=800.00E-18 Bf=843.08)
         .model  qx2  NPN(Is=800.0000E-18 Bf=843.08)
         .ends
```

```
* Schematics Subcircuit *
.subckt TLV2450_ver1 Vout Vdd GND V+ V– SD
*
        S_S2     $N_0001 GND SD GND S2
        RS_S2    SD GND 1G
        .MODEL S2 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
       + Von=1.0
        S_S1     $N_0002 VDD SD GND S1
        RS_S1    SD GND 1G
        .MODEL S1 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
       + Von=1.0
        S_S3     Vout $N_0003 SD GND S3
        RS_S3    SD GND 1G
        .MODEL S3 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
       + Von=1.0
        X_SUB_U1     V+ V– $N_0002 $N_003
       + AMP_TLV2450-X
        .ENDS    tlv2450_ver1
```

```
* Schematics Subcircuit *
.subckt TLV2451_ver1 V+ V– Vout Vdd GND
*
        X_SUB_U1     V+ V– GND Vout AMP_TLV2450-X
        .ENDS    tlv2451_ver1
```

Figure 49. Boyle Macromodel and Subcircuit

TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS220E – JULY 1998 – REVISED JUNE 1999

- **Input Common-Mode Range Exceeds Both Supply Rails . . . $V_{DD-} - 0.2V$ to $V_{DD+} + 0.2V$**
- **Gain Bandwidth Product . . . 6.4MHz**
- **Supply Current . . . 500µA/channel**
- **Input Offset Voltage . . . 100 µV**
- **Input Noise Voltage . . . 11nV/√Hz**
- **Rail-to-Rail Output Swing**
- **Slew Rate . . . 1.6 V/µs**
- **±90mA Output Drive Capability**
- **Micropower Shutdown Mode (TLV2460/3/5) . . . 0.3 µA/channel**
- **Available in 5- or 6-pin SOT23 and 8- or 10-Pin MSOP**
- **Characterized From T_A = –40°C to 125°C**
- **Universal Op Amp EVM**

TLV2460
DBV PACKAGE
(TOP VIEW)

OUT	1	6	V_{DD+}
GND	2	5	$\overline{SHDN}$
IN+	3	4	IN–

description

The TLV246x is a family of low-power rail-to-rail input/output operational amplifiers specifically designed for portable applications. The input common-mode voltage range extends beyond the supply rails for maximum dynamic range in low-voltage systems. The amplifier output has rail-to-rail performance with high-output-drive capability, solving one of the limitations of older rail-to-rail input/output operational amplifiers. This rail-to-rail dynamic range and high output drive make the TLV246x ideal for buffering analog-to-digital converters.

The operational amplifier has 6.4 MHz of bandwidth and 1.6 V/µs of slew rate with only 500 µA of supply current, providing good ac performance with low power consumption. Three members of the family offer a shutdown terminal, which places the amplifier in an ultra-low supply current mode (I_{DD} = 0.3 µA/ch). While in shutdown, the operational-amplifier output is placed in a high-impedance state. DC applications are also well served with an input noise voltage of 11 nV/√Hz and input offset voltage of 100 µV.

This family is available in the low-profile SOT23, MSOP, and TSSOP packages. The TLV2460 is the first rail-to-rail input/output operational amplifier with shutdown available in the 6-pin SOT23, making it perfect for high-density circuits. The family is specified over an expanded temperature range (T_A = –40°C to 125°C) for use in industrial control and automotive systems.

FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2460	1	8	8	6	—	—	X	UNIV-OPAMP–2
TLV2461	1	8	8	5	—	—		UNIV-OPAMP–1
TLV2462	2	8	8	—	—	8		UNIV-OPAMP–1
TLV2463	2	14	14	—	—	10†	X	UNIV-OPAMP–2
TLV2464	4	14	14	—	14	—		—
TLV2465	4	16	16	—	16	—	X	—

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

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TLV2460 and TLV2461 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM‡ (Y)
		SMALL OUTLINE (D)	SOT-23† (DBV)	PLASTIC DIP (P)	
0°C to 70°C	2000 µV	TLV2460CD TLV2461CD	TLV2460CDBV TLV2461CDBV	TLV2460CP TLV2461CP	TLV2460Y TLV2461Y
−40°C to 125°C	2000 µV	TLV2460ID TLV2461ID	TLV2460IDBV TLV2461IDBV	TLV2460IP TLV2461IP	— —
	1500 µV	TLV2460AID TLV2461AID	— —	TLV2460AIP TLV2461AIP	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2460CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2462 and TLV2463 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM‡ (Y)
		SMALL OUTLINE† (D)	MSOP (DGK)	MSOP† (DGS)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	2000 µV	TLV2462CD TLV2463CD	TLV2462CDGK —	— TLV2463CDGS	— TLV2463CN	TLV2462CP —	TLV2462Y TLV2463Y
−40°C to 125°C	2000 µV	TLV2462ID TLV2463ID	TLV2462IDGK —	— TLV2463IDGS	— TLV2463IN	TLV2462IP —	— —
	1500 µV	TLV2462AID TLV2463AID	— —	— —	— TLV2463AIN	TLV2462AIP —	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2462CDR).
‡ Chip forms are tested at T_A = 25°C only.

TLV2464 and TLV2465 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES			CHIP FORM‡ (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
0°C to 70°C	2000 µV	TLV2464CD TLV2465CD	TLV2464CN TLV2465CN	TLV2464CPW TLV2465CPW	TLV2464Y TLV2465Y
−40°C to 125°C	2000 µV	TLV2464ID TLV2465ID	TLV2464IN TLV2465IN	TLV2464IPW TLV2465IPW	— —
−40°C to 125°C	1500 µV	TLV2464AID TLV2465AID	TLV2464AIN TLV2465AIN	TLV2464AIPW TLV2465AIPW	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2464CDR).
‡ Chip forms are tested at T_A = 25°C only.

SOT-23 AND MSOP DEVICE SYMBOLS

DEVICE TYPE	NO. OF TERMINALS	PACKAGE NAME	SYMBOL
SOT-23	6 Pin	TLV2460CDBV	VAOC
		TLV2460IDBV	VAOI
	5 Pin	TLV2461CDBV	VAPC
		TLV2461IDBV	VAPI
MSOP	8 Pin	TLV2462CDGK	xxTIAAI
		TLV2462IDGK	xxTIAAJ
	10 Pin	TLV2463CDGS	xxTIAAK
		TLV2463IDGS	xxTIAAL

TLV246x PACKAGE PINOUTS

TLV2460
DBV PACKAGE
(TOP VIEW)

OUT	1	6	V$_{DD}$+
GND	2	5	$\overline{SHDN}$
IN+	3	4	IN−

TLV2461
DBV PACKAGE
(TOP VIEW)

OUT	1	5	V$_{DD}$+
GND	2		
IN+	3	4	IN−

TLV2462
D, DGK, OR P PACKAGE
(TOP VIEW)

1OUT	1	8	V$_{DD}$+
1IN−	2	7	2OUT
1IN+	3	6	2IN−
GND	4	5	2IN+

TLV2460
D OR P PACKAGE
(TOP VIEW)

NC	1	8	$\overline{SHDN}$
IN−	2	7	V$_{DD}$+
IN+	3	6	OUT
GND	4	5	NC

TLV2461
D OR P PACKAGE
(TOP VIEW)

NC	1	8	NC
IN−	2	7	V$_{DD}$+
IN+	3	6	OUT
GND	4	5	NC

TLV2463
DGS PACKAGE
(TOP VIEW)

1OUT	1	10	V$_{DD}$+
1IN−	2	9	2OUT
1IN+	3	8	2IN−
GND	4	7	2IN+
$\overline{1SHDN}$	5	6	$\overline{2SHDN}$

TLV2463
D OR N PACKAGE
(TOP VIEW)

1OUT	1	14	V$_{DD}$+
1IN−	2	13	2OUT
1IN+	3	12	2IN−
GND	4	11	2IN+
NC	5	10	NC
$\overline{1SHDN}$	6	9	$\overline{2SHDN}$
NC	7	8	NC

TLV2464
D, N, OR PWP PACKAGE
(TOP VIEW)

1OUT	1	14	4OUT
1IN−	2	13	4IN−
1IN+	3	12	4IN+
V$_{DD}$+	4	11	GND
2IN+	5	10	3IN+
2IN−	6	9	3IN−
2OUT	7	8	3OUT

TLV2465
D, N, OR PWP PACKAGE
(TOP VIEW)

1OUT	1	16	4OUT
1IN−	2	15	4IN−
1IN+	3	14	4IN+
V$_{DD}$+	4	13	GND
2IN+	5	12	3IN+
2IN−	6	11	3IN−
2OUT	7	10	3OUT
$\overline{1/2SHDN}$	8	9	$\overline{3/4SHDN}$

NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 6 V
Differential input voltage, V_{ID} . . . . V_{DD} – 0.2 V to V_{DD} + 0.2 V
Input current, I_I (any input) . . . . ± 200 mA
Output current, I_O . . . . ± 175 mA
Total input current, I_I (into V_{DD+}) . . . . 175 mA
Total output current, I_O (out of V_{DD-}) . . . . 175 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
I suffix . . . . –40°C to 125°C
Maximum junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD} –.

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
D (8)	38.3	176	725 mW
D (14)	26.9	122.6	725 mW
D (16)	25.7	114.7	725 mW
DBV (5)	55	324.1	437 mW
DBV (6)	55	294.3	437 mW
DGK	54.23	259.96	424 mW
DGS	54.1	257.71	424 mW
N (14)	32	78	1150 mW
N (16)	32	78	1150 mW
P	41	104	1000 mW
PW (14)	29.3	173.6	700 mW
PW (16)	28.7	161.4	700 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		V_{DD-}	V_{DD+}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV246x			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage (TLV246x)	$V_{DD} = \pm1.5$ V, $V_{IC} = 0$,	$V_O = 0$, $R_S = 50\ \Omega$	25°C		100	2000	μV
				Full range			2200	
α_{VIO}	Temperature coefficient of input offset voltage					2		μV/°C
I_{IO}	Input offset current	$V_{DD} = \pm1.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$		25°C		2.8	7	nA
			TLV246xC	Full range			20	
			TLV246xI	Full range			75	
I_{IB}	Input bias current			25°C		4.4	14	nA
			TLV246xC	Full range			25	
			TLV246xI	Full range			75	
V_{ICR}	Common-mode input voltage range	CMRR > 66 dB	$R_S = 50\ \Omega$	25°C	−0.2 to 3.2			V
		CMRR > 60 dB	$R_S = 50\ \Omega$	Full range	−0.2 to 3.2			
V_{OH}	High-level output voltage	$I_{OH} = -2.5$ mA		25°C	2.9			V
				Full range	2.8			
		$I_{OH} = -10$ mA		25°C	2.7			
				Full range	2.5			
V_{OL}	Low-level output voltage	$V_{IC} = 1.5$ V,	$I_{OL} = 2.5$ mA	25°C		0.1		V
				Full range			0.2	
		$V_{IC} = 1.5$ V,	$I_{OL} = 10$ mA	25°C		0.3		
				Full range			0.5	
I_{OS}	Short-circuit output current	Sourcing		25°C		50		mA
				Full range	20			
		Sinking		25°C		40		
				Full range	20			
I_O	Output current			25°C		±30		mA
A_{VD}	Large-signal differential voltage amplification	$R_L = 10$ kΩ		25°C	90	105		dB
				Full range	89			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz,	$A_V = 10$	25°C		33		Ω
CMRR	Common-mode rejection ratio	$V_{ICR} = -0.2$ V to 3.2 V, $R_S = 50\ \Omega$		25°C	66	80		dB
			TLV246xC	Full range	64			
			TLV246xI	Full range	60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} /\Delta V_{IO}$)	$V_{DD} = 2.7$ V to 6 V, No load	$V_{IC} = V_{DD}/2$,	25°C	80	85		dB
				Full range	75			
		$V_{DD} = 3$ V to 5 V, No load	$V_{IC} = V_{DD}/2$,	25°C	85	95		
				Full range	80			
I_{DD}	Supply current (per channels)	$V_O = 1.5$ V, $\overline{SHDN} > 1.02$ V	No load,	25°C		0.5	0.575	mA
				Full range			0.9	

† Full range is 0°C to 70°C for the C suffix and −40°C to 125°C for the I suffix. If not specified, full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV246x			UNIT
					MIN	TYP	MAX	
$V_{(ON)}$	Turnon voltage level	$A_V = 1$	Channel 1	25°C		1.021		V
			Channel 2			1.02		
$V_{(OFF)}$	Turnoff voltage level	$A_V = 1$	Channel 1	25°C		0.822		V
			Channel 2			0.817		
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463, TLV2465)	$\overline{SHDN}$ < 0.8 V, Per channel in shutdown		25°C		0.3		µA
				Full range			2.5	

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV246x			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)} = 2$ V, $R_L = 10$ kΩ	$C_L = 160$ pF,	25°C	1	1.6		V/µs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		16		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = 2$ V, $R_L = 10$ kΩ, f = 1 kHz	$A_V = 1$	25°C		0.006%		
			$A_V = 10$			0.02%		
			$A_V = 100$			0.08%		
$t_{(on)}$	Amplifier turnon time	$A_V = 1$, $R_L = 10$ kΩ	Both channels	25°C		7.6		µs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		
$t_{(off)}$	Amplifier turnoff time	$A_V = 1$, $R_L = 10$ kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, $C_L = 160$ pF	$R_L = 10$ kΩ,	25°C		5.2		MHz
t_s	Settling time	$V_{(STEP)PP} = 2$ V, $A_V = -1$, $C_L = 10$ pF, $R_L = 10$ kΩ	0.1%	25°C		1.47		µs
			0.01%			1.78		
		$V_{(STEP)PP} = 2$ V, $A_V = -1$, $C_L = 56$ pF, $R_L = 10$ kΩ	0.1%			1.77		
			0.01%			1.98		
ϕ_m	Phase margin at unity gain	$R_L = 10$ kΩ,	$C_L = 160$ pF	25°C		44°		
	Gain margin			25°C		7		dB

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV246x			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage (TLV246x)	V_{DD} = ±2.5 V, V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		150	2000	μV
				Full range			2200	
V_{IO}	Input offset voltage (TLV246xA)			25°C		150	1500	μV
				Full range			1700	
α_{VIO}	Temperature coefficient of input offset voltage			25°C		2		μV/°C
I_{IO}	Input offset current	V_{DD} = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		0.3	7	nA
			TLV246xC	Full range			15	
			TLV246xI	Full range			60	
I_{IB}	Input bias current			25°C		1.3	14	nA
			TLV246xC	Full range			30	
			TLV246xI	Full range			60	
V_{ICR}	Common-mode input voltage range	CMRR > 71 dB,	R_S = 50 Ω	25°C	−0.2 to 5.2			V
		CMRR > 60 dB,	R_S = 50 Ω	Full range	0 to 5			
V_{OH}	High-level output voltage	I_{OH} = −2.5 mA		25°C		4.9		V
				Full range	4.8			
		I_{OH} = −10 mA		25°C		4.8		
				Full range	4.7			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 2.5 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 10 mA	25°C		0.2		
				Full range			0.3	
I_{OS}	Short-circuit output current	Sourcing		25°C		145		mA
				Full range	60			
		Sinking		25°C		100		
				Full range	60			
I_O	Output current			25°C		±90		mA
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,	25°C	92	109		dB
				Full range	90			
$r_{i(d)}$	Differential input resistance			25°C		10^9		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		7		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		29		Ω
CMRR	Common-mode rejection ratio	V_{ICR} = −0.2 V to 5.2 V, R_S = 50 Ω		25°C	71	85		dB
			TLV246xC	Full range	69			
			TLV246xI	Full range	60			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	80	85		dB
				Full range	75			
		V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	85	95		dB
				Full range	80			

† Full range is 0°C to 70°C for the C suffix and −40°C to 125°C for the I suffix. If not specified, full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV246x			UNIT
					MIN	TYP	MAX	
I_{DD}	Supply current (per channel)	V_O = 2.5 V, $\overline{SHDN}$ > 1.38 V	No load,	25°C		0.55	0.65	mA
				Full range			1	
$V_{(ON)}$	Turnon voltage level	A_V = 1	Channel 1	25°C		1.372		V
			Channel 2			1.368		
$V_{(OFF)}$	Turnoff voltage level	A_V = 1	Channel 1	25°C		1.315		V
			Channel 2			1.309		
$I_{DD(SHDN)}$	Supply current in shutdown (TLV2460, TLV2463, TLV2465)	$\overline{SHDN}$ < 1.3 V, Per channels in shutdown		25°C		1		μA
				Full range			3	

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV246x			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 160 pF,	25°C	1	1.6		V/μs
				Full range	0.8			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz		25°C		11		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.13		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V, R_L = 10 kΩ, f = 10 kHz	A_V = 1	25°C		0.004%		
			A_V = 10			0.01%		
			A_V = 100			0.04%		
$t_{(on)}$	Amplifier turnon time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		7.6		μs
			Channel 1 only, Channel 2 on			7.65		
			Channel 2 only, Channel 1 on			7.25		
$t_{(off)}$	Amplifier turnoff time	A_V = 1, R_L = 10 kΩ	Both channels	25°C		333		ns
			Channel 1 only, Channel 2 on			328		
			Channel 2 only, Channel 1 on			329		
	Gain-bandwidth product	f = 10 kHz, C_L = 160 pF	R_L = 10 kΩ,	25°C		6.4		MHz
t_S	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.53		μs
			0.01%			1.83		
		$V_{(STEP)PP}$ = 2 V, A_V = –1, C_L = 56 pF, R_L = 10 kΩ	0.1%			3.13		
			0.01%			3.33		
φm	Phase margin at unity gain	R_L = 10 kΩ,	C_L = 160 pF	25°C		45°		
	Gain margin			25°C		7		dB

† Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

TYPICAL CHARACTERISTICS

Table of Graphs

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TLV2460, TLV2461, TLV2462, TLV2463, TLV2464, TLV2465
FAMILY OF LOW-POWER RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS220E – JULY 1998 – REVISED JUNE 1999

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

$V_{DD} = 3$ V
$T_A = 25°C$

Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

$V_{DD} = 5$ V
$T_A = 25°C$

Figure 2

INPUT BIAS AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

$V_{DD} = 3$ V
$V_I = 1.5$ V

Figure 3

INPUT BIAS AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

$V_{DD} = 5$ V
$V_I = 2.5$ V

Figure 4

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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 6

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 8

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

V_{DD} = 3 V
A_V = –10
THD = 1%
R_L = 10 kΩ

Figure 9

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

V_{DD} = 5 V
A_V = –10
THD = 1%
R_L = 10 kΩ

Figure 10

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

V_{DD} = ±1.5 V
R_L = 10 kΩ
C_L = 0
T_A = 25°C

A_{VD}

Phase

Figure 11

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TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

Figure 12

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

Figure 13

AMPLIFER STABILITY
vs
LOAD

Figure 14

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 15

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 16

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 17

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TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 18

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 19

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 20

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 21

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TYPICAL CHARACTERISTICS

**AMPLIFIER WITH A SHUTDOWN PULSE
TURNON CHARACTERISTICS**

Figure 22

**AMPLIFIER WITH A SHUTDOWN PULSE
TURNOFF CHARACTERISTICS**

Figure 23

**SUPPLY CURRENT WITH A SHUTDOWN PULSE
TURNON CHARACTERISTICS**

Figure 24

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TYPICAL CHARACTERISTICS

TURNOFF SUPPLY CURRENT
WITH A SHUTDOWN PULSE

Figure 25

SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 26

SLEW RATE
vs
SUPPLY VOLTAGE

Figure 27

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

$V_{DD} = 3$ V
$A_V = 10$
$V_I = 1.5$ V
$T_A = 25°C$

Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

$V_{DD} = 5$ V
$A_V = 10$
$V_I = 2.5$ V
$T_A = 25°C$

Figure 29

EQUIVALENT INPUT NOISE VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

$V_{DD} = 3$ V
$A_V = 10$
$f = 1$ kHz
$T_A = 25°C$

Figure 30

EQUIVALENT INPUT NOISE VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

$V_{DD} = 5$ V
$A_V = 10$
$f = 1$ kHz
$T_A = 25°C$

Figure 31

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TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

$V_{DD} = \pm 1.5$ V
$V_{O(PP)} = 2$ V
$R_L = 10$ kΩ

$A_V = 100$
$A_V = 10$
$A_V = 1$

THD – Total Harmonic Distortion – %

f – Frequency – Hz

Figure 32

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

$V_{DD} = \pm 2.5$ V
$V_{O(PP)} = 4$ V
$R_L = 10$ kΩ

$A_V = 100$
$A_V = 10$
$A_V = 1$

THD – Total Harmonic Distortion – %

f – Frequency – Hz

Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
PEAK-TO-PEAK SIGNAL AMPLITUDE

$V_{DD} = 3$ V
$A_V = 1$
$T_A = 25°C$

$R_L = 250$ Ω
$R_L = 2$ kΩ
$R_L = 10$ kΩ
$R_L = 100$ kΩ

THD+N – Total Harmonic Distortion +Noise – %

Peak-to-Peak Signal Amplitude – V

Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
PEAK-TO-PEAK SIGNAL AMPLITUDE

$R_L = 250$ Ω
$R_L = 2$ kΩ
$R_L = 10$ kΩ
$R_L = 100$ kΩ

$V_{DD} = 5$ V
$A_V = 1$
$T_A = 25°C$

THD+N – Total Harmonic Distortion +Noise – %

Peak-to-Peak Signal Amplitude – V

Figure 35

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TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 36

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

Figure 37

GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

Figure 38

GAIN BANDWIDTH PRODUCT
vs
FREE-AIR TEMPERATURE

Figure 39

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TYPICAL CHARACTERISTICS

LARGE SIGNAL FOLLOWER

$V_{DD} = 3$ V
$V_{I(PP)} = 1$ V
$V_I = 1.5$ V
$R_L = 10$ kΩ
$C_L = 160$ pF
$A_V = 1$
$T_A = 25°C$

Figure 40

LARGE SIGNAL FOLLOWER

$V_{DD} = 5$ V
$V_{I(PP)} = 2$ V
$V_I = 2.5$ V
$R_L = 10$ kΩ
$C_L = 160$ pF
$A_V = 1$
$T_A = 25°C$

Figure 41

SMALL SIGNAL FOLLOWER

$V_{DD} = 3$ V
$V_{I(PP)} = 100$ mV $C_L = 160$ pF
$V_I = 1.5$ V $A_V = 1$
$R_L = 10$ kΩ $T_A = 25°C$

Figure 42

SMALL SIGNAL FOLLOWER

$V_{DD} = 5$ V
$V_{I(PP)} = 100$ mV $C_L = 160$ pF
$V_I = 2.5$ V $A_V = 1$
$R_L = 10$ kΩ $T_A = 25°C$

Figure 43

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TYPICAL CHARACTERISTICS

INVERTING LARGE SIGNAL

V_{DD} = 3 V
$V_{I(PP)}$ = 1 V
V_I = 1.5 V
R_L = 10 kΩ
C_L = 160 pF
A_V = –1
T_A = 25°C

Input

Output

Figure 44

INVERTING LARGE SIGNAL

V_{DD} = 5 V
$V_{I(PP)}$ = 2 V
V_I = 2.5 V
R_L = 10 kΩ
C_L = 160 pF
A_V = –1
T_A = 25°C

Input

Output

Figure 45

INVERTING SMALL SIGNAL

V_{DD} = 3 V
$V_{I(PP)}$ = 100 mV
V_I = 1.5 V
R_L = 10 kΩ
C_L = 160 pF
A_V = –1
T_A = 25°C

Input

Output

Figure 46

INVERTING SMALL SIGNAL

V_{DD} = 5 V
$V_{I(PP)}$ = 100 mV
V_I = 2.5 V
R_L = 10 kΩ
C_L = 160 pF
A_V = –1
T_A = 25°C

Input

Output

Figure 47

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APPLICATION INFORMATION

shutdown function

Three members of the TLV246x family (TLV2460/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.3 µA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 22, 23, 24, and 25. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 48 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS246x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = $\theta_{JC} + \theta_{CA}$
$\quad\quad\theta_{JC}$ = Thermal coefficient from junction to case
$\quad\quad\theta_{CA}$ = Thermal coefficient from case to ambient air (°C/W)

APPLICATION INFORMATION

general power dissipation considerations (continued)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

NOTE A.   Results are with no air flow and using JEDEC Standard Low-K test PCB.
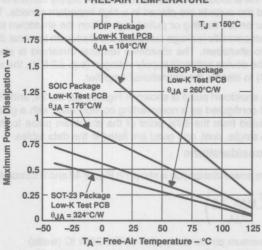
Figure 48. Maximum Power Dissipation vs Free-Air Temperature

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 48 are generated using the TLV246x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
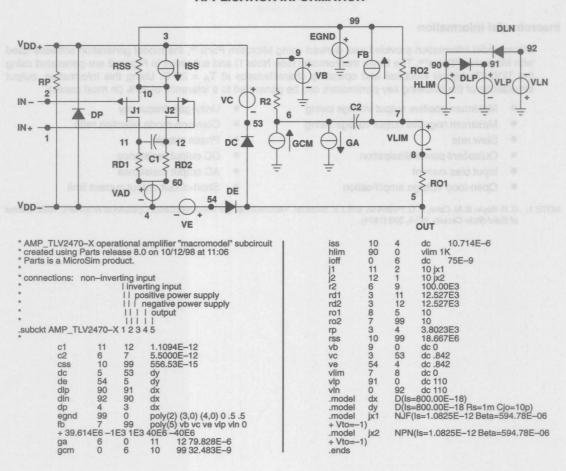- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2:   G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

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APPLICATION INFORMATION

macromodel information (continued)


```
.SUBCKT TLV246X   1 2 3 4 5
      C1      11    12    2.46034E–12
      C2      6     7     10.0000E–12
      CSS     10    99    443.21E–15
      DC      5     53    DY
      DE      54    5     DY
      DLP     90    91    DX
      DLN     92    90    DX
      DP      4     3     DX
      EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
      FB      7     99    POLY (5) VB VC VE VLP
  +   VLN 0 21.600E6 –1E3 1E3 22E6 –22E6
      GA      6     0     11    12 345.26E–6
      GCM     0     6     10    99 15.4226E–9
      ISS     10    4     DC 18.850E–6
      HLIM    90    0     VLIM 1K
      J1      11    2     10 JX1
      J2      12    1     10 JX2
      R2      6     9     100.00E3
```

```
      RD1     3     11    2.8964E3
      RD2     3     12    2.8964E3
      R01     8     5     5.6000
      R02     7     99    6.2000
      RP      3     4     8.9127
      RSS     10    99    10.610E6
      VB      9     0     DC 0
      VC      3     53    DC .7836
      VE      54    4     DC .7436
      VLIM    7     8     DC 0
      VLP     91    0     DC 117
      VLN     0     92    DC 117
      .MODEL DX D (IS=800.00E–18)
      .MODEL DY D (IS=800.00E–18 Rs = 1m Cjo=10p)
      .MODEL JX1 NJF (IS=1.0000E–12 BETA=6.3239E–3
  +   VTO=–1)
      .MODEL JX2 NJF (IS=1.0000E–12 BETA=6.3239E–3
  +   VTO=–1)
      .ENDS
```

Figure 49. Boyle Macromodels and Subcircuit

macromodel information (continued)
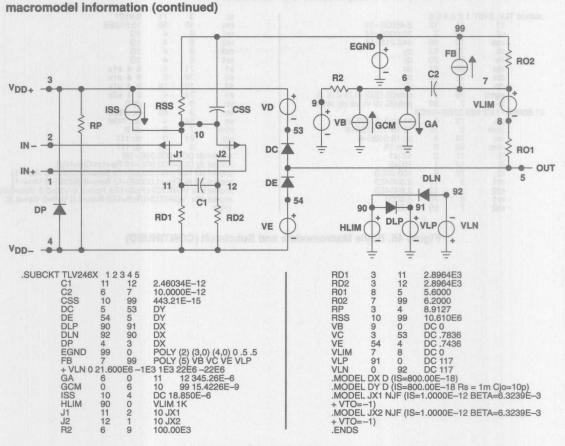
```
.subckt TLV_246Y 1 2 3 4 5 6                          rp      3    71   8.9127
        c1      11    12   2.4603E–12                 rss    10    99   10.610E6
        c2      72    7    10.000E–12                 rs1     6    4    1G
        css     10    99   443.21E–15                 rs2     6    4    1G
        dc      70    53   dy                         rs3     6    4    1G
        de      54    70   dy                         rs4     6    4    1G
        dlp     90    91   dx                         s1     71    4    6 4 s1x
        dln     92    90   dx                         s2     70    5    6 4 s1x
        dp      4     3    dx                         s3     10    74   6 4 s1x
        egnd    99    0    poly(2) (3,0) (4,0) 0 .5 .5  s4   74    4    6 4 s2x
        fb      7     99   poly(5) vb vc ve vlp vln 0 vb      9    0    dc 0
21.600E6 –1E3 1E3 22E6 –22E6                          vc      3    53   dc .7836
        ga      72    0    11 12 345.26E–6            ve     54    4    dc .7436
        gcm     0     72   10 99 15.422E–9            vlim    7    8    dc 0
        iss     74    4    dc 18.850E–6               vlp    91    0    dc 117
        hlim    90    0    vlim 1K                    vln     0    92   dc 117
        j1      11    2    10 jx1                    .model dx D(Is=800.00E–18)
        j2      12    1    10 jx2                    .model dy D(Is=800.00E–18 Rs=1m Cjo=10p)
        r2      72    9    100.00E3                  .model jx1 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
        rd1     3     11   2.8964E3                  .model jx2 NJF(Is=1.0000E–12 Beta=6.3239E–3 Vto=–1)
        rd2     3     12   2.8964E3                  .model s1x VSWITCH(Roff=1E8 Ron=1.0 Voff=2.5 Von=0.0)
        ro1     8     70   5.6000                    .model s2x VSWITCH(Roff=1E8 Ron=1.0 Voff=0 Von=2.5)
        ro2     7     99   6.2000                    .ends
```

Figure 48. Boyle Macromodels and Subcircuit (CONTINUED)

TEXAS
INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TLV2470, TLV2471, TLV2472, TLV2473, TLV2474, TLV2475, TLV247xA
FAMILY OF 600-μA/Ch 2.8-MHz RAIL-TO-RAIL INPUT/OUTPUT
HIGH-DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS232A – JUNE 1999 – REVISED AUGUST 1999

- **CMOS Rail-To-Rail Input/Output**
- **Input Bias Current . . . 2.5 pA**
- **Low Supply Current . . . 600 μA/Channel**
- **Ultra-Low Power Shutdown Mode**
  $I_{DD(SHDN)}$ . . . 350 nA/ch at 3 V
  $I_{DD(SHDN)}$ . . . 1000 nA/ch at 5 V
- **Gain-Bandwidth Product . . . 2.8 MHz**
- **High Output Drive Capability**
  - **±10 mA at 180 mV**
  - **±35 mA at 500 mV**
- **Input Offset Voltage . . . 250 μV (typ)**
- **Supply Voltage Range . . . 2.7 V to 6 V**
- **Ultra-Small Packaging**
  - **5 or 6 Pin SOT-23 (TLV2470/1)**
  - **8 or 10 Pin MSOP (TLV2472/3)**

TLV2470
DBV† PACKAGE
(TOP VIEW)

```
          ┌─────┐
OUT  [ 1  │     │  6 ]  VDD+
GND  [ 2  │  ▷  │  5 ]  SHDN
IN+  [ 3  │     │  4 ]  IN–
          └─────┘
```

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

description

The TLV247x is a family of CMOS rail-to-rail input/output operational amplifiers that establishes a new performance point for supply current versus ac performance. These devices consume just 600 μA/channel while offering 2.8 MHz of gain bandwidth product. Along with increased ac performance, the amplifier provides high output drive capability, solving a major shortcoming of older micropower operational amplifiers. The TLV247x can swing to within 180 mV of each supply rail while driving a 10-mA load. For non-RRO applications, the TLV247x can supply ±35 mA at 500 mV off the rail. Both the inputs and outputs swing rail-to-rail for increased dynamic range in low-voltage applications. This performance makes the TLV247x family ideal for sensor interface, portable medical equipment, and other data acquisition circuits.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2470	1	8	8	6‡	—	—	Yes	UNIV-OPAMP–2
TLV2471	1	8	8	5‡	—	—	—	UNIV-OPAMP–1
TLV2472	2	8	8	—	—	8	—	UNIV-OPAMP–1
TLV2473	2	14	14	—	—	10	Yes	UNIV-OPAMP–2
TLV2474	4	14	14	—	14‡	—	—	—
TLV2475	4	16	16	—	16‡	—	Yes	—

‡ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS§

DEVICE	V_{DD} (V)	BW (MHz)	SLEW RATE (V/μs)	I_{DD} (per channel) (μA)	RAIL-TO-RAIL
TLV247X	2.7 – 6.0	2.8	1.5	600	I/O
TLV245X	2.7 – 6.0	0.22	0.11	23	I/O
TLV246X	2.7 – 6.0	6.4	1.6	550	I/O
TLV277X	2.5 – 6.0	5.1	10.5	1000	O

§ All specifications measured at 5 V.

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TLV2470, TLV2471, TLV2472, TLV2473, TLV2474, TLV2475, TLV247xA
FAMILY OF 600-μA/Ch 2.8-MHz RAIL-TO-RAIL INPUT/OUTPUT
HIGH-DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS232A – JUNE 1999 – REVISED AUGUST 1999

TLV2470 and TLV2471 AVAILABLE OPTIONS

T$_A$	PACKAGED DEVICES					CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	SOT-23		PLASTIC DIP (P)		
		(DBV)†	SYMBOL			
0°C to 70°C	TLV2470CD TLV2471CD	TLV2470CDBV§ TLV2471CDBV§	VAUC VAVC	TLV2470CP TLV2471CP		TLV2470Y TLV2471Y
−40°C to 125°C	TLV2470ID TLV2471ID	TLV2470IDBV§ TLV2471IDBV§	VAUI VAVI	TLV2470IP TLV2471IP		— —
	TLV2470AID TLV2471AID	— —	— —	TLV2470AIP TLV2471AIP		— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2470CDR).
‡ Chip forms are tested at T$_A$ = 25°C only.
§ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

TLV2472 AND TLV2473 AVAILABLE OPTIONS

T$_A$	PACKAGED DEVICES					PLASTIC DIP (N)	PLASTIC DIP (P)	CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	MSOP		MSOP				
		(DGN)†	SYMBOL§	(DGQ)†	SYMBOL§			
0°C to 70°C	TLV2472CD TLV2473CD	TLV2472CDGN —	xxTIABU —	— TLV2473CDGQ	— xxTIABW	— TLV2473CN	TLV2472CP —	TLV2472Y TLV2473Y
−40°C to 125°C	TLV2472ID TLV2473ID	TLV2472IDGN —	xxTIABV —	— TLV2473IDGQ	— xxTIABX	— TLV2473IN	TLV2472IP —	— —
	TLV2472AID TLV2473AID	— —	— —	— —	— —	— TLV2473AIN	TLV2472AIP —	— —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2472CDR).
‡ Chip forms are tested at T$_A$ = 25°C only.
§ xx represents the device date code.

TLV2474 and TLV2475 AVAILABLE OPTIONS

T$_A$	PACKAGED DEVICES				CHIP FORM‡ (Y)
	SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PW)†	TSSOP (PWP)†	
0°C to 70°C	TLV2474CD TLV2475CD	TLV2474CN TLV2475CN	TLV2475CPW	TLV2474CPWP§	TLV2474Y TLV2475Y
−40°C to 125°C	TLV2474ID TLV2475ID	TLV2474IN TLV2475IN	TLV2475IPW	TLV2475CPWP§	— —
	TLV2474AID TLV2475AID	TLV2474AIN TLV2475AIN	TLV2475AIPW	TLV2475CPWP§	— —
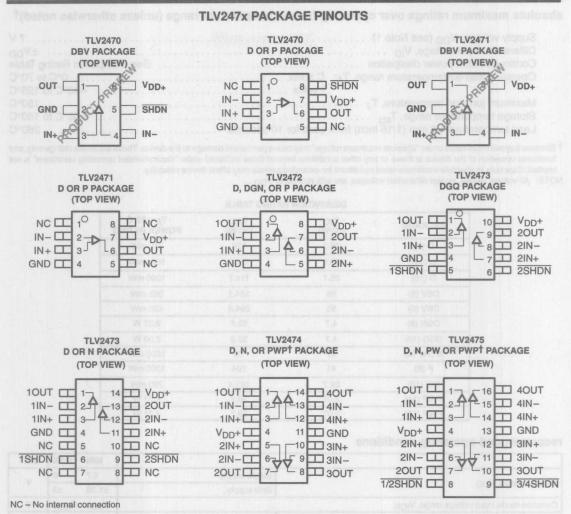
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2474CDR).
‡ Chip forms are tested at T$_A$ = 25°C only.
§ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

TEXAS INSTRUMENTS

TLV247x PACKAGE PINOUTS

TLV2470
DBV PACKAGE
(TOP VIEW)

OUT 1	V_DD+
GND 2	5 SHDN
IN+ 3	4 IN−

TLV2470
D OR P PACKAGE
(TOP VIEW)

NC 1	8 SHDN
IN− 2	7 V_DD+
IN+ 3	6 OUT
GND 4	5 NC

TLV2471
DBV PACKAGE
(TOP VIEW)

OUT 1	V_DD+
GND 2	5
IN+ 3	4 IN−

TLV2471
D OR P PACKAGE
(TOP VIEW)

NC 1	8 NC
IN− 2	7 V_DD+
IN+ 3	6 OUT
GND 4	5 NC

TLV2472
D, DGN, OR P PACKAGE
(TOP VIEW)

1OUT 1	8 V_DD+
1IN− 2	7 2OUT
1IN+ 3	6 2IN−
GND 4	5 2IN+

TLV2473
DGQ PACKAGE
(TOP VIEW)

1OUT 1	10 V_DD+
1IN− 2	9 2OUT
1IN+ 3	8 2IN−
GND 4	7 2IN+
1SHDN 5	6 2SHDN

TLV2473
D OR N PACKAGE
(TOP VIEW)

1OUT 1	14 V_DD+
1IN− 2	13 2OUT
1IN+ 3	12 2IN−
GND 4	11 2IN+
NC 5	10 NC
1SHDN 6	9 2SHDN
NC 7	8 NC

TLV2474
D, N, OR PWP† PACKAGE
(TOP VIEW)

1OUT 1	14 4OUT
1IN− 2	13 4IN−
1IN+ 3	12 4IN+
V_DD+ 4	11 GND
2IN+ 5	10 3IN+
2IN− 6	9 3IN−
2OUT 7	8 3OUT

TLV2475
D, N, PW OR PWP† PACKAGE
(TOP VIEW)

1OUT 1	16 4OUT
1IN− 2	15 4IN−
1IN+ 3	14 4IN+
V_DD+ 4	13 GND
2IN+ 5	12 3IN+
2IN− 6	11 3IN−
2OUT 7	10 3OUT
1/2SHDN 8	9 3/4SHDN

NC – No internal connection

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

description (continued)

Three members of the family (TLV2470/3/5) offer a shutdown terminal for conserving battery life in portable applications. During shutdown, the outputs are placed in a high-impedance state and the amplifier consumes only 350 nA/channel. The family is fully specified at 3 V and 5 V across an expanded industrial temperature range (−40°C to 125°C). The singles and duals are available in the SOT23 and MSOP packages, while the quads are available in TSSOP. The TLV2470 offers an amplifier with shutdown functionality all in a 6-pin SOT23 package, making it perfect for high density power-sensitive circuits.

TLV2470, TLV2471, TLV2472, TLV2473, TLV2474, TLV2475, TLV247xA
FAMILY OF 600-µA/Ch 2.8-MHz RAIL-TO-RAIL INPUT/OUTPUT
HIGH-DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN
SLOS232A – JUNE 1999 – REVISED AUGUST 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1) . . . . 7 V
Differential input voltage, V_{ID} . . . . $\pm V_{DD}$
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . 0°C to 70°C
                I suffix . . . . −40°C to 125°C
Maximum junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to V_{DD-}.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGN (8)	4.7	52.7	2.37 W
DGQ (10)	4.7	52.3	2.39 W
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (16)	28.7	161.4	720 mW
PWP (14)	2.07	30.7	4.07 W
PWP (16)	2.07	29.7	4.21 W

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply	2.7	6	V
	Split supply	±1.35	±3	
Common-mode input voltage range, V_{ICR}		V_{DD-}	V_{DD+}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	−40	125	

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV247x		25°C		250	2200	µV
				Full range			2400	
		TLV247xA		25°C		250	1600	
				Full range			1800	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω				0.4		µV/°C
I_{IO}	Input offset current			25°C		1.5	50	pA
			TLV247xC	Full range			100	
			TLV247xI	Full range			300	pA
I_{IB}	Input bias current			25°C		2	50	pA
			TLV247xC	Full range			100	
			TLV247xI	Full range			300	pA
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB	R_S = 50 Ω	25°C	−0.2 to 3.2			V
		CMRR > 52 dB	R_S = 50 Ω	Full range	−0.2 to 3.2			
V_{OH}	High-level output voltage	V_{IC} = 1.5 V	I_{OH} = −2.5 mA	25°C	2.85	2.94		V
				Full range	2.8			
			I_{OH} = −10 mA	25°C	2.6	2.74		
				Full range	2.5			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V	I_{OL} = 2.5 mA	25°C		0.07	0.15	V
				Full range			0.2	
			I_{OL} = 10 mA	25°C		0.2	0.35	
				Full range			0.4	
I_{OS}	Short-circuit output current	Sourcing		25°C	30			mA
				Full range	20			
		Sourcing, Outside of rails‡		25°C	62			
			TLV247xC	Full range	60			
			TLV247xI	Full range	59			
		Sinking		25°C	30			
				Full range	20			
		Sinking, Outside of rails‡		25°C	62			
			TLV247xC	Full range	60			
			TLV247xI	Full range	59			
I_O	Output current	V_O = 0.5 V from rail		25°C		±22		mA
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 1 V,	R_L = 10 kΩ	25°C	90	116		dB
				Full range	88			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		19.3		pF
z_O	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		2		Ω

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.
‡ Depending on package dissipation rating

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3 V, R_S = 50 Ω		25°C	61	78		dB
			TLV247xC	Full range	59			
			TLV247xI	Full range	58			
		V_{IC} = −0.2 to 3.2 V, R_S = 50 Ω, Outside of rails		25°C	62	78		
			TLV247xC	Full range	60			
			TLV247xI	Full range	59			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	74	90		dB
				Full range	66			
		V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	77	92		
				Full range	68			
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		550	750	µA
				Full range			800	
$V_{(ON)}$	Turnon voltage level	Relative to GND		25°C		1.03		V
$V_{(OFF)}$	Turnoff voltage level	Relative to GND		25°C		0.81		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2470, TLV2473, TLV2475) (per channel)	$\overline{SHDN}$ = < 1.45 V		25°C		350	1500	nA
			TLV247xC	Full range			2000	
			TLV247xI	Full range			4000	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	1.1	1.4		V/µs
				Full range	0.6			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		28		nV/√Hz
		f = 1 kHz		25°C		15		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.405		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.1%		
			A_V = 100			0.5%		
$t_{(on)}$	Amplifier turnon time	R_L = OPEN‡		25°C		5		µs
$t_{(off)}$	Amplifier turnoff time			25°C		250		ns
	Gain-bandwidth product	f = 10 kHz,	R_L = 600 Ω	25°C		2.8		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.5		µs
			0.01%			3.9		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.6		
			0.01%			4		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		61°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		15		dB

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.
‡ Depending on package dissipation rating

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV247x			25°C		250	2200	µV
					Full range			2400	
		TLV247xA			25°C		250	1600	
					Full range			2000	
α_{VIO}	Temperature coefficient of input offset voltage		$V_{DD} = \pm2.5$ V $V_{IC} = 0, \; V_O = 0,$ $R_S = 50 \; \Omega$				0.4		µV/°C
I_{IO}	Input offset current				25°C		1.7	50	pA
				TLV247xC	Full range			100	pA
				TLV247xI	Full range			300	pA
I_{IB}	Input bias current				25°C		2.5	50	pA
				TLV247xC	Full range			100	pA
				TLV247xI	Full range			300	pA
V_{ICR}	Common-mode input voltage range		CMRR > 70 dB	$R_S = 50 \; \Omega$	25°C	−0.2 to 5.2			V
			CMRR > 52 dB	$R_S = 50 \; \Omega$	Full range	−0.2 to 5.2			
V_{OH}	High-level output voltage		$V_{IC} = 2.5$ V	$I_{OH} = -2.5$ mA	25°C	4.85	4.96		V
					Full range	4.8			
				$I_{OH} = -10$ mA	25°C	4.72	4.82		
					Full range	4.65			
V_{OL}	Low-level output voltage		$V_{IC} = 2.5$ V	$I_{OL} = 2.5$ mA	25°C		0.07	0.15	V
					Full range			0.2	
				$I_{OL} = 10$ mA	25°C		0.178	0.28	
					Full range			0.35	
I_{OS}	Short-circuit output current		Sourcing		25°C	90			mA
					Full range	60			
			Sourcing, Outside of rails‡		25°C	63			
				TLV247xC	Full range	61			
				TLV247xI	Full range	58			
			Sinking		25°C	110			
					Full range	60			
			Sinking, Outside of rails‡		25°C	63			
				TLV247xC	Full range	61			
				TLV247xI	Full range	58			
I_O	Output current		$V_O = 0.5$ V from rail		25°C		±35		mA
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)} = 3$ V,	$R_L = 10 \; k\Omega$	25°C	92	120		dB
					Full range	91			
$r_{i(d)}$	Differential input resistance				25°C		10^{12}		Ω
C_{IC}	Common-mode input capacitance		$f = 10$ kHz		25°C		18.9		pF
z_O	Closed-loop output impedance		$f = 10$ kHz,	$A_V = 10$	25°C		1.8		Ω

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.
‡ Depending on package dissipation rating

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 5 V, R_S = 50 Ω		25°C	64	84		dB
			TLV247xC	Full range	63			
			TLV247xI	Full range	58			
		V_{IC} = −0.2 to 5.2 V, R_S = 50 Ω, Outside of rails		25°C	63	82		
			TLV247xC	Full range	61			
			TLV247xI	Full range	58			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	74	90		dB
				Full range	66			
		V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	77	92		
				Full range	66			
I_{DD}	Supply current (per channel)	V_O = 2.5 V,	No load	25°C		600	900	μA
				Full range			1000	
$V_{(ON)}$	Turnon voltage level	Relative to GND		25°C		1.38		V
$V_{(OFF)}$	Turnoff voltage level	Relative to GND		25°C		1.3		V
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2470, TLV2473, TLV2475) (per channel)	$\overline{SHDN}$ = < 1.45 V		25°C		1000	2500	nA
			TLV247xC	Full range			3000	
			TLV247xI	Full range			6000	nA

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)
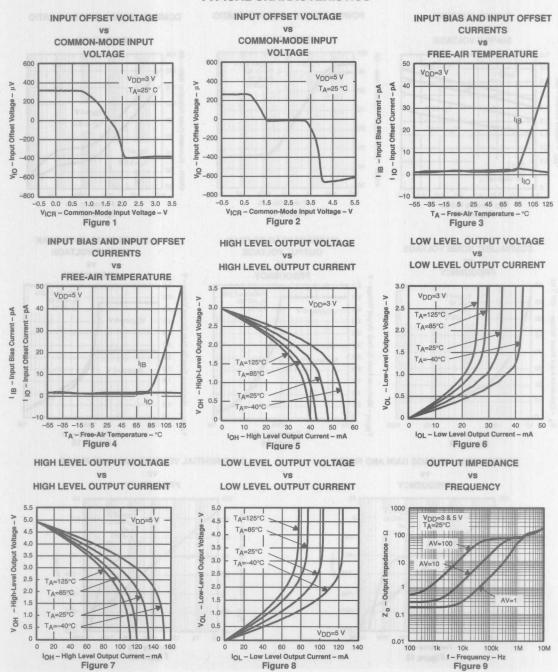
PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	1.1	1.5		V/μs
				Full range	0.7			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		28		nV/√Hz
		f = 1 kHz		25°C		15		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.39		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 4 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.01%		
			A_V = 10			0.05%		
			A_V = 100			0.3%		
$t_{(on)}$	Amplifier turnon time	R_L = OPEN‡		25°C		5		μs
$t_{(off)}$	Amplifier turnoff time			25°C		250		ns
	Gain-bandwidth product	f = 10 kHz,	R_L = 600 Ω	25°C		2.8		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		1.8		μs
			0.01%			3.3		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			1.7		
			0.01%			3		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		68°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		23		dB

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix. If not specified, full range is −40°C to 125°C.
‡ Disable and enable time are defined as the interval between application of logic signal to SHDN and the point at which the supply current has reached half its final value.

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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

Figure 2

INPUT BIAS AND INPUT OFFSET
CURRENTS
vs
FREE-AIR TEMPERATURE

Figure 3

INPUT BIAS AND INPUT OFFSET
CURRENTS
vs
FREE-AIR TEMPERATURE

Figure 4

HIGH LEVEL OUTPUT VOLTAGE
vs
HIGH LEVEL OUTPUT CURRENT

Figure 5

LOW LEVEL OUTPUT VOLTAGE
vs
LOW LEVEL OUTPUT CURRENT

Figure 6

HIGH LEVEL OUTPUT VOLTAGE
vs
HIGH LEVEL OUTPUT CURRENT

Figure 7

LOW LEVEL OUTPUT VOLTAGE
vs
LOW LEVEL OUTPUT CURRENT

Figure 8

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 9

TLV2470, TLV2471, TLV2472, TLV2473, TLV2474, TLV2475, TLV247xA
FAMILY OF 600-μA/Ch 2.8-MHz RAIL-TO-RAIL INPUT/OUTPUT
HIGH-DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS232A – JUNE 1999 – REVISED AUGUST 1999

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 10

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

Figure 11

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 12

EQUIVALENT NOISE VOLTAGE
vs
FREQUENCY

Figure 13

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

Figure 14

MAXIMUM PEAK-TO-PEAK
OUTPUT VOLTAGE
vs
FREQUENCY

Figure 15

DIFFERENTIAL VOLTAGE GAIN AND PHASE
vs
FREQUENCY

Figure 16

DIFFERENTIAL VOLTAGE GAIN AND PHASE
vs
FREQUENCY

Figure 17

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TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 18

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 19

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 20

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 21

GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

Figure 22

SLEW RATE
vs
SUPPLY VOLTAGE

Figure 23

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 24

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 25

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TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

Figure 26

TOTAL HARMONIC
DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 27

TOTAL HARMONIC
DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 28

LARGE SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME

Figure 29

LARGE SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME

Figure 30

SMALL SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME

Figure 31

SMALL SIGNAL FOLLOWER
PULSE RESPONSE
vs
TIME

Figure 32

SHUTDOWN (ON AND OFF)
PULSE RESPONSE
vs
TIME

Figure 33

SHUTDOWN (ON AND OFF)
PULSE RESPONSE
vs
TIME

Figure 34

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TYPICAL CHARACTERISTICS

SHUTDOWN FORWARD
ISOLATION
vs
FREQUENCY

Figure 35

SHUTDOWN REVERSE ISOLATION
vs
FREQUENCY

Figure 36

SHUTDOWN SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 37

SHUTDOWN SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 38

SHUTDOWN PULSE CURRENT
vs
TIME

Figure 39

SHUTDOWN PULSE CURRENT
vs
TIME

Figure 40

PARAMETER MEASUREMENT INFORMATION

Figure 41

APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 42. A minimum value of 20 Ω should work well for most applications.
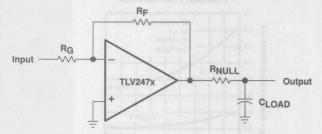
Figure 42. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$
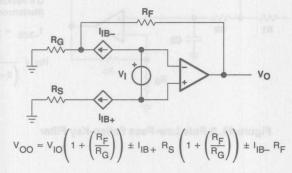
Figure 43. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 44).

$$f_{-3dB} = \frac{1}{2\pi R1 C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$
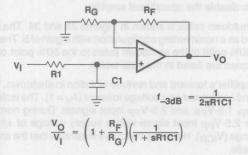
Figure 44. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

APPLICATION INFORMATION

general configurations (continued)

$R1 = R2 = R$
$C1 = C2 = C$
$Q = $ Peaking Factor
(Butterworth $Q = 0.707$)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$
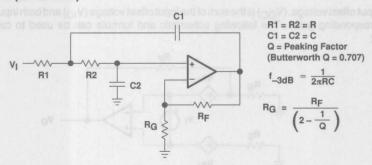
Figure 45. 2-Pole Low-Pass Sallen-Key Filter

shutdown function

Three members of the TLV247x family (TLV2470/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 350 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to V_{DD}– (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 33 and 34. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 35 and 36 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35-V supplies and configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency using 0.1-V_{PP}, 1.5-V_{PP}, and 2.5-V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.5-V_{PP} input signal with a supply voltage of ±1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

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APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV247x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.

- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.

- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

general PowerPAD™ design considerations

The TLV247x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 46(a) and Figure 46(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 46(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

Side View (a)

End View (b)

Bottom View (c)

Thermal
Pad

NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 46. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

Thermal Pad Area

Single or Dual

68 mils x 70 mils) with 5 vias
(Via diameter = 13 mils

Quad

78 mils x 94 mils) with 9 vias
(Via diameter = 13 mils)
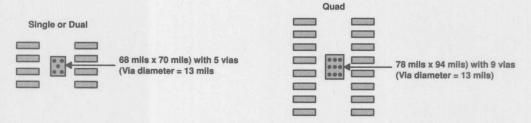
Figure 47. PowerPAD PCB Etch and Via Pattern

PowerPAD is a trademark of Texas Instruments Incorporated.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

1. Prepare the PCB with a top side etch pattern as shown in Figure 47. There should be etch for the leads as well as etch for the thermal pad.

2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLV247x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.

4. Connect all holes to the internal ground plane.

5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLV247x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the TLV247x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given θ_{JA}, the maximum power dissipation is shown in Figure 48 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of TLV247x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

TEXAS INSTRUMENTS

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

PWP Package
Low-K Test PCB
$\theta_{JA} = 29.7°C/W$

$T_J = 150°C$

SOT-23 Package
Low-K Test PCB
$\theta_{JA} = 324°C/W$

DGN Package
Low-K Test PCB
$\theta_{JA} = 52.3°C/W$

SOIC Package
Low-K Test PCB
$\theta_{JA} = 176°C/W$

PDIP Package
Low-K Test PCB
$\theta_{JA} = 104°C/W$

Maximum Power Dissipation – W

T_A – Free-Air Temperature – °C

NOTE A. Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 48. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially muti-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 49 to Figure 54 show this effect, along with the quiescent heat, with an ambient air temperature of 70°C and 125°C. When using $V_{DD} = 3$ V, there is generally not a heat problem with an ambient air temperature of 70°C. But, when using $V_{DD} = 5$ V, the packages are severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

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APPLICATION INFORMATION

general PowerPAD design considerations (continued)

TLV2470, TLV2471†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

Figure 49

TLV2470, TLV2471†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

Figure 50

TLV2472, TLV2473†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

Figure 51

TLV2472, TLV2473†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

Figure 52
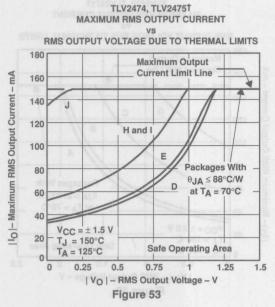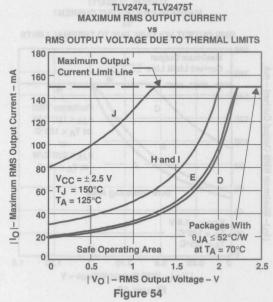
† A – SOT23(5); B – SOT23 (6); C – SOIC (8); D – SOIC (14); E – SOIC (16); F – MSOP PP (8); G – PDIP (8); H – PDIP (14); I – PDIP (16);
J – TSSOP PP (14/16)

APPLICATION INFORMATION
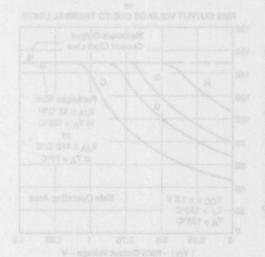
general PowerPAD design considerations (continued)

TLV2474, TLV2475†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

Figure 53

TLV2474, TLV2475†
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

Figure 54

† A – SOT23(5); B – SOT23 (6); C – SOIC (8); D – SOIC (14); E – SOIC (16); F – MSOP PP (8); G – PDIP (8); H – PDIP (14); I – PDIP (16);
J – TSSOP PP (14/16)

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 2 are generated using the TLV247x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1:   G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

Figure 2. Boyle Macromodel and Subcircuit

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APPLICATION INFORMATION


```
* AMP_TLV2470–X operational amplifier "macromodel" subcircuit
* created using Parts release 8.0 on 10/12/98 at 11:06
* Parts is a MicroSim product.
*
* connections:   non–inverting input
*                 I inverting input
*                 I I positive power supply
*                 I I I negative power supply
*                 I I I I output
*                 I I I I I
.subckt AMP_TLV2470–X 1 2 3 4 5
*
        c1      11      12      1.1094E–12
        c2      6       7       5.5000E–12
        css     10      99      556.53E–15
        dc      5       53      dy
        de      54      5       dy
        dlp     90      91      dx
        dln     92      90      dx
        dp      4       3       dx
        egnd    99      0       poly(2) (3,0) (4,0) 0 .5 .5
        fb      7       99      poly(5) vb vc ve vlp vln 0
+ 39.614E6 –1E3 1E3 40E6 –40E6
        ga      6       0       11      12 79.828E–6
        gcm     0       6       10      99 32.483E–9
```

```
        iss     10      4       dc      10.714E–6
        hlim    90      0       vlim 1K
        ioff    0       6       dc      75E–9
        j1      11      2       10 jx1
        j2      12      1       10 jx2
        r2      6       9       100.00E3
        rd1     3       11      12.527E3
        rd2     3       12      12.527E3
        ro1     8       5       10
        ro2     7       99      10
        rp      3       4       3.8023E3
        rss     10      99      18.667E6
        vb      9       0       dc 0
        vc      3       53      dc .842
        ve      54      4       dc .842
        vlim    7       8       dc 0
        vlp     91      0       dc 110
        vln     0       92      dc 110
        .model  dx      D(Is=800.00E–18)
        .model  dy      D(Is=800.00E–18 Rs=1m Cjo=10p)
        .model  jx1     NJF(Is=1.0825E–12 Beta=594.78E–06
+ Vto=–1)
        .model  jx2     NPN(Is=1.0825E–12 Beta=594.78E–06
+ Vto=–1)
        .ends
```

```
* Schematics Subcircuit *
.subckt TLV2470_ver1 Vout Vdd GND V+ V– SD
*
        S_S2    $N_0001 GND SD GND S2
        RS_S2   SD GND 1G
        .MODEL S2 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
        + Von=1.0
        S_S1    $N_0002 VDD SD GND S1
        RS_S1   SD GND 1G
        .MODEL S1 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
        + Von=1.0
        S_S3    Vout $N_0003 SD GND S3
        RS_S3   SD GND 1G
        .MODEL S3 VSWITCH Roff=1e6 Ron=1.0 Voff=0.0
        + Von=1.0
        X_SUB_U1        V+ V– $N_0002 $N_003
        + AMP_TLV2470–X
        .ENDS   TLV2470_ver1
```

```
* Schematics Subcircuit *
.subckt TLV2471_ver1 V+ V– Vout Vdd GND
*
        X_SUB_U1        V+ V– GND Vout AMP_TLV2470–X
        .ENDS   TLV2471_ver1
```

Figure 55. Boyle Macromodel and Subcircuit
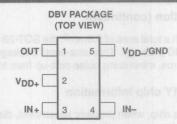
- Output Swing Includes Both Supply Rails
- Low Noise . . . 21 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Very Low Power . . . 11 μA Per Channel Typ
- Common-Mode Input Voltage Range Includes Negative Rail
- Wide Supply Voltage Range 2.7 V to 10 V
- Available in the SOT-23 Package
- Macromodel Included

DBV PACKAGE
(TOP VIEW)

```
OUT  [ 1      5 ]  V_DD_/GND
V_DD+ [ 2          ]
IN+  [ 3      4 ]  IN–
```
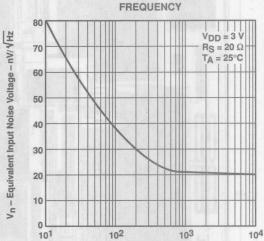
description

The TLV2711 is a single low-voltage operational amplifier available in the SOT-23 package. It consumes only 11 μA (typ) of supply current and is ideal for battery-power applications. Looking at Figure 1, the TLV2711 has a 3-V noise level of 21 nV/√Hz at 1kHz; five times lower than competitive SOT-23 micropower solutions. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2711 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2711, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

Figure 1. Equivalent Input Noise Voltage Versus Frequency

AVAILABLE OPTIONS

T_A	V_IO max AT 25°C	PACKAGED DEVICES SOT-23 (DBV)†	SYMBOL	CHIP FORM‡ (Y)
0°C to 70°C	3 mV	TLV2711CDBV	VAJC	TLV2711Y
–40°C to 85°C	3 mV	TLV2711IDBV	VAJI	

† The DBV package available in tape and reel only.
‡ Chip forms are tested at T_A = 25°C only.

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TLV2711, TLV2711Y
Advanced LinCMOS™ RAIL-TO-RAIL
MICROPOWER SINGLE OPERATIONAL AMPLIFIERS

SLOS196 – AUGUST 1997
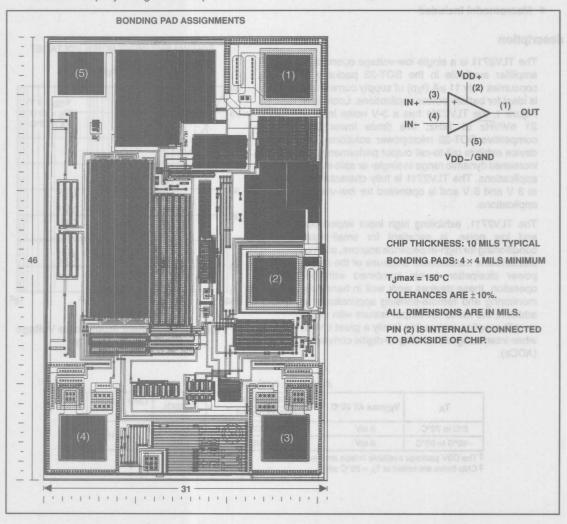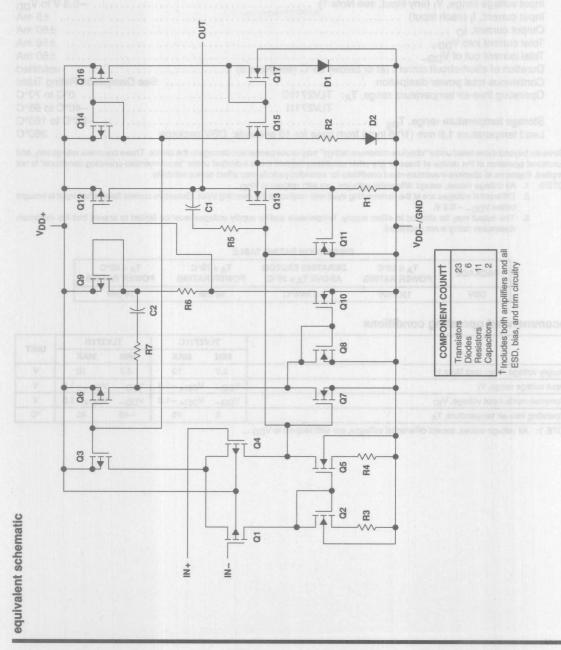
description (continued)

With a total area of 5.6mm^2, the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

TLV2711Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2711C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

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equivalent schematic

OUT

IN+

IN–

$V_{DD}+$

$V_{DD}-/GND$

Q16 Q14 Q12 Q9 Q3 Q6 Q17 Q15 Q13 Q11 Q10 Q8 Q7 Q5 Q2 Q4 Q1

D1 D2

R1 R2 R3 R4 R5 R6 R7

C1 C2

COMPONENT COUNT†	
Transistors	23
Diodes	6
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 12 V
Differential input voltage, V_{ID} (see Note 2) .... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) .... −0.3 V to V_{DD}
Input current, I_I (each input) .... ±5 mA
Output current, I_O .... ±50 mA
Total current into V_{DD+} .... ±50 mA
Total current out of V_{DD-} .... ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) .... unlimited
Continuous total power dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A: TLV2711C .... 0°C to 70°C
⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀⠀TLV2711I .... −40°C to 85°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2711C		TLV2711I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

electrical characteristics at specified free-air temperature, $V_{DD} = 3$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2711C MIN	TYP	MAX	TLV2711I MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			Full range		0.4	3		0.4	3	mV
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD\pm} = \pm1.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$	Full range		1			1		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			Full range		0.5	150		0.5	150	pA
I_{IB}	Input bias current			Full range		1	150		1	150	pA
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le 5$ mV,	$R_S = 50\ \Omega$	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	$I_{OH} = -100$ µA		25°C		2.94			2.94		V
		$I_{OH} = -250$ µA		25°C		2.85			2.85		
				Full range	2.6			2.6			
V_{OL}	Low-level output voltage	$V_{IC} = 1.5$ V,	$I_{OL} = 50$ µA	25°C		15			15		mV
		$V_{IC} = 1.5$ V,	$I_{OL} = 500$ µA	25°C		150			150		
				Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 1.5$ V, $V_O = 1$ V to 2 V	$R_L = 10$ kΩ‡	25°C	3	7		3	7		V/mV
				Full range	1			1			
			$R_L = 1$ MΩ‡	25°C		600			600		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz,		25°C		5			5		pF
z_o	Closed-loop output impedance	$f = 7$ kHz,	$A_V = 1$	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 1.7 V, $R_S = 50\ \Omega$	$V_O = 1.5$ V,	25°C	65	83		65	83		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio $(\Delta V_{DD}/\Delta V_{IO})$	$V_{DD} = 2.7$ V to 8 V, No load	$V_{IC} = V_{DD}/2$	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	$V_O = 1.5$ V,	No load	25°C		11	25		11	25	µA
				Full range			30			30	

† Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is −40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150°C$ extrapolated to $T_A = 25°C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2711C			TLV2711I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, R_L = 10 kΩ‡, C_L = 100 pF‡		25°C	0.01	0.025		0.01	0.025		V/µs
				Full range	0.005			0.005			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		80			80		nV/√Hz
		f = 1 kHz		25°C		22			22		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		660			660		µV
		f = 0.1 Hz to 10 Hz		25°C		880			880		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 10 kΩ‡,	25°C		56			56		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 10 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		7			7		kHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		20			20		dB

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2711C MIN	TLV2711C TYP	TLV2711C MAX	TLV2711I MIN	TLV2711I TYP	TLV2711I MAX	UNIT
V_{IO}	Input offset voltage					0.45	3		0.45	3	mV
α_{VIO}	Temperature coefficient of input offset voltage			Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50\ \Omega$	25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq 5$ mV	$R_S = 50\ \Omega$	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	$I_{OH} = -100$ µA		25°C		4.95			4.95		V
		$I_{OH} = -250$ µA		25°C		4.875			4.875		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50$ µA	25°C		12			12		mV
		$V_{IC} = 2.5$ V,	$I_{OL} = 500$ µA	25°C		120			120		
				Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 10$ kΩ‡	25°C	6	12		6	12		V/mV
				Full range	3			3			
			$R_L = 1$ MΩ‡	25°C		800			800		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz,		25°C		5			5		pF
z_o	Closed-loop output impedance	$f = 7$ kHz,	$A_V = 1$	25°C		200			200		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $R_S = 50\ \Omega$	$V_O = 2.5$ V,	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 8 V, No load	$V_{IC} = V_{DD}/2$,	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	$V_O = 2.5$ V,	No load	25°C		13	25		13	25	µA
				Full range			30			30	

† Full range for the TLV2711C is 0°C to 70°C. Full range for the TLV2711I is − 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150$°C extrapolated to $T_A = 25$°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A[†]	TLV2711C MIN	TLV2711C TYP	TLV2711C MAX	TLV2711I MIN	TLV2711I TYP	TLV2711I MAX	UNIT
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, R_L = 10 kΩ[‡], C_L = 100 pF[‡]	25°C	0.01	0.025		0.01	0.025		V/µs
			Full range	0.005			0.005			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		72			72		nV/√Hz
		f = 1 kHz	25°C		21			21		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz	25°C		600			600		µV
		f = 0.1 Hz to 10 Hz	25°C		800			800		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ[‡], C_L = 100 pF[‡]	25°C		65			65		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 10 kΩ[‡], A_V = 1, C_L = 100 pF[‡]	25°C		7			7		kHz
ϕ_m	Phase margin at unity gain	R_L = 10 kΩ[‡], C_L = 100 pF[‡]	25°C		60°			60°		
	Gain margin		25°C		22			22		dB

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			TLV2711Y MIN	TLV2711Y TYP	TLV2711Y MAX	UNIT
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, R_S = 50 Ω	V_O = 0,	V_{IC} = 0,		0.47		mV
I_{IO}	Input offset current					0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\mid V_{IO} \mid \leq 5$ mV,	R_S = 50 Ω			–0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = –100 µA				2.94		V
		I_{OH} = –200 µA				2.85		
V_{OL}	Low-level output voltage	V_{IC} = 0,	I_{OL} = 50 µA			15		mV
		V_{IC} = 0,	I_{OL} = 500 µA			150		
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V,	V_O = 1 V to 2 V	R_L = 10 kΩ[†]		7		V/mV
				R_L = 1 MΩ[†]		600		
$r_{i(d)}$	Differential input resistance					10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance					10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz				5		pF
z_o	Closed-loop output impedance	f = 7 kHz,	A_V = 1			200		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 1.5 V,	R_S = 50 Ω		83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = $V_{DD}/2$,	No load		95		dB
I_{DD}	Supply current	V_O = 1.5 V,	No load			11		µA

† Referenced to 1.5 V

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electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2711Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm = \pm2.5$ V, $R_S = 50$ Ω	$V_{IC} = 0$,	$V_O = 0$,		0.45		mV
I_{IO}	Input offset current					0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\mid V_{IO} \mid \leq 5$ mV,	$R_S = 50$ Ω		−0.3 to 4.2			V
V_{OH}	High-level output voltage	$I_{OH} = -100$ μA				4.95		V
		$I_{OH} = -250$ μA				4.875		
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 50$ μA			12		mV
		$V_{IC} = 2.5$ V,	$I_{OL} = 500$ μA			120		
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V,	$V_O = 1$ V to 4 V	$R_L = 10$ kΩ†		12		V/mV
				$R_L = 1$ MΩ†		800		
$r_{i(d)}$	Differential input resistance					10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance					10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz				5		pF
z_o	Closed-loop output impedance	f = 7 kHz,	$A_V = 1$			200		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V,	$V_O = 2.5$ V,	$R_S = 50$ Ω		83		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 8 V,	$V_{IC} = V_{DD}/2$,	No load		95		dB
I_{DD}	Supply current	$V_O = 2.5$ V,	No load			13		μA

† Referenced to 1.5 V

TYPICAL CHARACTERISTICS

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		vs Frequency	23, 24
		vs Free-air temperature	25, 26
z_o	Output impedance	vs Frequency	27, 28
CMRR	Common-mode rejection ratio	vs Frequency	29
		vs Free-air temperature	30
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	31, 32
		vs Free-air temperature	33
I_{DD}	Supply current	vs Supply voltage	34
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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2711
INPUT OFFSET VOLTAGE**

546 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 1.5$ V
$T_A = 25°C$

Figure 2

**DISTRIBUTION OF TLV2711
INPUT OFFSET VOLTAGE**

376 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 2.5$ V
$T_A = 25°C$

Figure 3

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

$V_{DD} = 3$ V
$R_S = 50$ Ω
$T_A = 25°C$

Figure 4

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

$V_{DD} = 5$ V
$R_S = 50$ Ω
$T_A = 25°C$
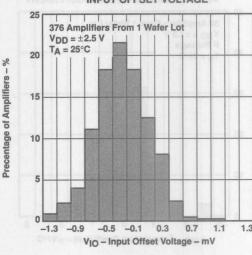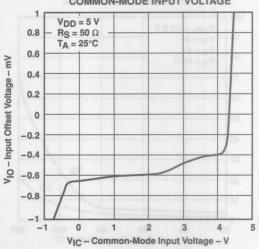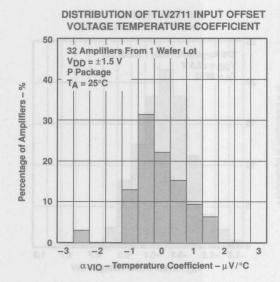
Figure 5

† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2711 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

Figure 6

DISTRIBUTION OF TLV2711 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT

Figure 7

INPUT BIAS AND INPUT OFFSET CURRENTS†
vs
FREE-AIR TEMPERATURE

Figure 8

INPUT VOLTAGE
vs
SUPPLY VOLTAGE

Figure 9

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE†‡
vs
FREE-AIR TEMPERATURE

Figure 10

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 11

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 12

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 14

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 15

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡
vs
FREQUENCY

Figure 16

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†‡
vs
FREE-AIR TEMPERATURE

Figure 18

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 19

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION‡
vs
LOAD RESISTANCE

Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†
vs
FREQUENCY

Figure 22

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN†
vs
FREQUENCY

Figure 23

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

Figure 24

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

Figure 25

OUTPUT IMPEDANCE‡
vs
FREQUENCY

Figure 26

OUTPUT IMPEDANCE‡
vs
FREQUENCY

Figure 27

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO[†]
vs
FREQUENCY

Figure 28

COMMON-MODE REJECTION RATIO[†][‡]
vs
FREE-AIR TEMPERATURE

Figure 29

SUPPLY-VOLTAGE REJECTION RATIO[†]
vs
FREQUENCY

Figure 30

SUPPLY-VOLTAGE REJECTION RATIO[†]
vs
FREQUENCY

Figure 31

[†] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
[‡] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

$V_{DD} = 2.7$ V to 8 V
$V_{IC} = V_O = V_{DD}/2$

Figure 32

SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

$V_O = V_{DD}/2$
$V_{IC} = V_{DD}/2$
No Load

$T_A = -40°C$
$T_A = 25°C$
$T_A = 85°C$

Figure 33

SLEW RATE‡
vs
LOAD CAPACITANCE

$V_{DD} = 5$ V
$A_V = -1$
$T_A = 25°C$

SR–
SR+

Figure 34

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

$V_{DD} = 5$ V
$R_L = 10$ kΩ
$C_L = 100$ pF
$A_V = 1$

SR–
SR+

Figure 35

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

$V_{DD} = 3\ V$
$R_L = 10\ k\Omega$
$C_L = 100\ pF$
$A_V = -1$
$T_A = 25°C$

V_O – Output Voltage – V

t – Time – μs

Figure 36

INVERTING LARGE-SIGNAL PULSE RESPONSE†

$V_{DD} = 5\ V$
$R_L = 10\ k\Omega$
$C_L = 100\ pF$
$A_V = -1$
$T_A = 25°C$

V_O – Output Voltage – V

t – Time – μs

Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

$V_{DD} = 5\ V$
$R_L = 10\ k\Omega$
$C_L = 100\ pF$
$A_V = 1$
$T_A = 25°C$

V_O – Output Voltage – V

t – Time – μs

Figure 38

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

$V_{DD} = 5\ V$
$C_L = 100\ pF$
$A_V = 1$
$T_A = 25°C$

$R_L = 100\ k\Omega$
Tied to 2.5 V

$R_L = 10\ k\Omega$
Tied to 2.5 V

$R_L = 10\ k\Omega$
Tied to 0 V

V_O – Output Voltage – V

t – Time – μs

Figure 39

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE†

V_{DD} = 3 V
R_L = 10 kΩ
C_L = 100 pF
A_V = −1
T_A = 25°C

Figure 40

INVERTING SMALL-SIGNAL PULSE RESPONSE†

V_{DD} = 5 V
R_L = 10 kΩ
C_L = 100 pF
A_V = −1
T_A = 25°C

Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

V_{DD} = 3 V
R_L = 10 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

Figure 42

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

V_{DD} = 5 V
R_L = 10 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

Figure 44

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

Figure 45

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD†

Figure 46

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY

Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

V_{DD} = 5 V
f = 10 kHz
R_L = 10 kΩ
C_L = 100 pF

Gain-Bandwidth Product – kHz

T_A – Free-Air Temperature – °C

Figure 48

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

R_L = 10 kΩ
C_L = 100 pF
T_A 25°C

Gain-Bandwidth Product – kHz

V_{DD} – Supply Voltage – V

Figure 49

PHASE MARGIN
vs
LOAD CAPACITANCE

T_A = 25°C

ϕ_m – Phase Margin

R_{null} = 1000 Ω

R_{null} = 500 Ω

R_{null} = 0

10 kΩ
10 kΩ
V_I
V_{DD+}
R_{null}
V_{DD-}
C_L

C_L – Load Capacitance – pF

Figure 50

GAIN MARGIN
vs
LOAD CAPACITANCE

R_{null} = 1000 Ω

R_{null} = 500 Ω

Gain Margin – dB

R_{null} = 0

T_A = 25°C

C_L – Load Capacitance – pF

Figure 51

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

Figure 52

APPLICATION INFORMATION

driving large capacitive loads

The TLV2711 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 50 and Figure 51 illustrate its ability to drive loads up to 600 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 53) improves the gain and phase margins when driving large capacitive loads. Figure 50 and Figure 51 show the effects of adding series resistances of 500 Ω and 1000 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right) \qquad (1)$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

APPLICATION INFORMATION

driving large capacitive loads (continued)

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 52). To use equation 1, UGBW must be approximated from Figure 52.
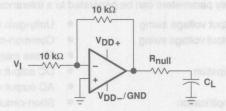
Figure 53. Series-Resistance Circuit

driving heavy dc loads

The TLV2711 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 µA and source 250 µA at V_{DD} = 3 V and V_{DD} = 5 V at a maximum quiescent I_{DD} of 25 µA. This provides a greater than 90% power efficiency.

When driving heavy dc loads, such as 10 kΩ, the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 38. This condition is affected by three factors.

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 39 illustrates two 10-kΩ load conditions. The first load condition shows the distortion seen for a 10-kΩ load tied to 2.5 V. The third load condition shows no distortion for a 10-kΩ load tied to 0 V.

- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 39 illustrates the difference seen on the output for a 10-kΩ load and a 100-kΩ load with both tied to 2.5 V.

- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 54 are generated using the TLV2711 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).


```
.SUBCKT TLV2711 1 2 3 4 5
        C1      11      12      8.86E–12
        C2      6       7       50.00E–12
        DC      5       53      DX
        DE      54      5       DX
        DLP     90      91      DX
        DLN     92      90      DX
        DP      4       3       DX
        EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
        FB      7       99      POLY (5) VB VC VE VLP
        + VLN 0 4.29E6 –6E6 6E6 6E6 –6E6
        GA      6       0       11      12 9.425E–6
        GCM     0       6       10      99 1320.2E–12
        ISS     3       10      DC 1.250E–6
        HLIM    90      0       VLIM 1K
        J1      11      2       10 JX
        J2      12      1       10 JX
        R2      6       9       100.0E3

        RD1     60      11      106.1E3
        RD2     60      12      106.1E3
        R01     8       5       50
        R02     7       99      150
        RP      3       4       419.2E3
        RSS     10      99      160.0E6
        VAD     60      4       –.5
        VB      9       0       DC 0
        VC      3       53      DC .55
        VE      54      4       DC .55
        VLIM    7       8       DC 0
        VLP     91      0       DC 0.1
        VLN     0       92      DC 2.6
        .MODEL DX D (IS=800.0E–18)
        .MODEL JX PJF (IS=500.0E–15 BETA=166E–6
        + VTO=–.004)
        .ENDS
```

Figure 54. Boyle Macromodel and Subcircuit

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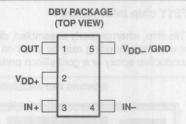
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/$\sqrt{Hz}$ Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Very Low Power . . . 110 μA Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**

DBV PACKAGE
(TOP VIEW)

OUT	1	5	V$_{DD-}$/GND
V$_{DD+}$	2		
IN+	3	4	IN–

description

The TLV2721 is a single low-voltage operational amplifier available in the SOT-23 package. It offers a compromise between the ac performance and output drive of the TLV2731 and the micropower TLV2711.

It consumes only 150 μA (max) of supply current and is ideal for battery-powered applications. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLV2721 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2721, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs).

With a total area of 5.6mm^2, the SOT-23 package only requires one third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

AVAILABLE OPTIONS

T$_A$	V$_{IO}$max AT 25°C	PACKAGED DEVICES	SYMBOL	CHIP FORM‡ (Y)
		SOT-23 (DBV)†		
0°C to 70°C	3 mV	TLV2721CDBV	VAKC	TLV2721Y
−40°C to 85°C	3 mV	TLV2721IDBV	VAKI	

† The DBV package available in tape and reel only.
‡ Chip forms are tested at T$_A$ = 25°C only.
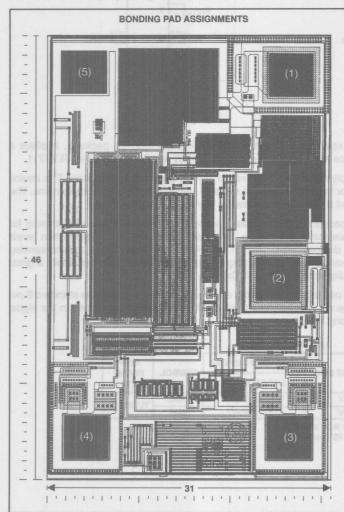
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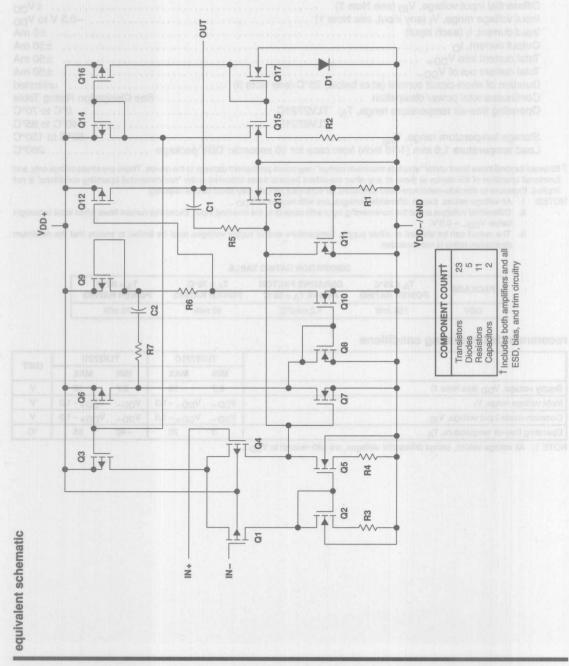
TLV2721, TLV2721Y
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS

TLV2721Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2721C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic

OUT

Q16 Q17 D1

Q14 Q15 R2

Q12 C1 Q13 R1

V_DD+ R5 Q11 V_DD–/GND

Q9 R6 Q10

C2 Q8

R7

Q6 Q7

Q3 Q4 Q5 R4

Q2 R3

Q1

IN+

IN–

COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	−0.3 V to V_{DD}
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of $V_{DD−}$	±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TLV2721C	0°C to 70°C
TLV2721I	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to $V_{DD−}$.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD−} − 0.3$ V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2721C		TLV2721I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	$V_{DD−}$	$V_{DD+} − 1.3$	$V_{DD−}$	$V_{DD+} − 1.3$	V
Common-mode input voltage, V_{IC}	$V_{DD−}$	$V_{DD+} − 1.3$	$V_{DD−}$	$V_{DD+} − 1.3$	V
Operating free-air temperature, T_A	0	70	−40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to $V_{DD−}$.

TEXAS INSTRUMENTS

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electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2721C			TLV2721I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage			Full range		0.5	3		0.5	3	mV
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1			1		µV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD}\pm = \pm1.5$ V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$|V_{IO}| \leq 5$ mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	$I_{OH} = -100$ µA		25°C		2.97			2.97		V
		$I_{OH} = -400$ µA		25°C		2.88			2.88		
				Full range	2.6			2.6			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		15			15		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		150			150		
				Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 2 kΩ‡	25°C	2	3		2	3		V/mV
				Full range	1			1			
			R_L = 1 MΩ‡	25°C		250			250		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz		25°C		6			6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		90			90		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	70	82		70	82		dB
				Full range	65			65			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 1.5 V,	No load	25°C		100	150		100	150	µA
				Full range			200			200	

† Full range for the TLV2721C is 0°C to 70°C. Full range for the TLV2721I is − 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2721, TLV2721Y
Advanced LinCMOS™ RAIL-TO-RAIL
VERY LOW-POWER SINGLE OPERATIONAL AMPLIFIERS
SLOS197 – AUGUST 1997

operating characteristics at specified free-air temperature, V_{DD} = 3 V

	PARAMETER	TEST CONDITIONS		T_A†	TLV2721C			TLV2721I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, R_L = 2 kΩ‡, C_L = 100 pF‡		25°C	0.1	0.25		0.1	0.25		V/µs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		120			120		nV/√Hz
		f = 1 kHz		25°C		20			20		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		680			680		mV
		f = 0.1 Hz to 10 Hz		25°C		860			860		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 1 V to 2 V, f = 20 kHz, R_L = 2 kΩ‡	A_V = 1	25°C		2.52%			2.52%		
			A_V = 10			7.01%			7.01%		
		V_O = 1 V to 2 V, f = 20 kHz, R_L = 2 kΩ§	A_V = 1	25°C		0.076%			0.076%		
			A_V = 10			0.147%			0.147%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 2 kΩ‡,	25°C		480			480		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 2 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		30			30		kHz
t_s	Settling time	A_V = –1, Step = 1 V to 2 V, R_L = 2 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		4.5			4.5		µs
			To 0.01%	25°C		6.8			6.8		µs
ϕ_m	Phase margin at unity gain	R_L = 2 kΩ‡,	C_L = 100 pF‡	25°C		53°			53°		
	Gain margin			25°C		12			12		dB

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V
§ Referenced to 0 V

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2721C			TLV2721I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage					0.5	3		0.5	3	mV
α_{VIO}	Temperature coefficient of input offset voltage			Full range		1			1		µV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD}\pm$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$|V_{IO}| \leq$ 5 mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −500 µA		25°C	4.75	4.88		4.75	4.88		V
		I_{OH} = −1 mA			4.6	4.76		4.6	4.76		
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		12			12		mV
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		120			120		
				Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 2 kΩ‡	25°C	3	5		3	5		V/mV
				Full range	1			1			
			R_L = 1 MΩ‡	25°C		800			800		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz		25°C		6			6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10	25°C		70			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	70	85		70	85		dB
				Full range	65			65			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			
I_{DD}	Supply current	V_O = 2.5 V,	No load	25°C		110	150		110	150	µA
				Full range			200			200	

† Full range for the TLV2721C is 0°C to 70°C. Full range for the TLV2721I is – 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD} = 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLV2721C			TLV2721I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5$ V to 3.5 V, $C_L = 100$ pF‡	$R_L = 2$ kΩ‡,	25°C	0.1	0.25		0.1	0.25		V/μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		90			90		nV/√Hz
		f = 1 kHz		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		800			800		mV
		f = 0.1 Hz to 10 Hz		25°C		960			960		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	$V_O = 1.5$ V to 3.5 V, f = 20 kHz, $R_L = 2$ kΩ‡	$A_V = 1$	25°C		2.45%			2.45%		
			$A_V = 10$			5.54%			5.54%		
		$V_O = 1.5$ V to 3.5 V, f = 20 kHz, $R_L = 2$ kΩ§	$A_V = 1$	25°C		0.142%			0.142%		
			$A_V = 10$			0.257%			0.257%		
	Gain-bandwidth product	f = 1 kHz, $C_L = 100$ pF‡	$R_L = 2$ kΩ‡,	25°C		510			510		kHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 1$ V, $R_L = 2$ kΩ‡,	$A_V = 1$, $C_L = 100$ pF‡	25°C		40			40		kHz
t_S	Settling time	$A_V = -1$, Step = 1.5 V to 3.5 V, $R_L = 2$ kΩ‡, $C_L = 100$ pF‡	To 0.1%	25°C		6.8			6.8		μs
			To 0.01%	25°C		9.2			9.2		
ϕ_m	Phase margin at unity gain	$R_L = 2$ kΩ‡,	$C_L = 100$ pF‡	25°C		53°			53°		
	Gain margin			25°C		12			12		dB

† Full range is −40°C to 85°C.
‡ Referenced to 2.5 V
§ Referenced to 0 V

electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2721Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V,	V_{IC} = 0,	V_O = 0,		620		µV
I_{IO}	Input offset current	R_S = 50 Ω				0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le$ 5 mV,	R_S = 50 Ω			−0.3 to 2.2		V
V_{OH}	High-level output voltage	I_{OH} = −100 µA				2.97		V
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA			15		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA			150		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 2 V	R_L = 2 kΩ†			3		V/mV
			R_L = 1 MΩ†			250		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10			90		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω		82		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load		95		dB
I_{DD}	Supply current	V_O = 0,		No load		100		µA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			TLV2721Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V,	V_{IC} = 0,	V_O = 0,		610		µV
I_{IO}	Input offset current	R_S = 50 Ω				0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$\lvert V_{IO}\rvert \le$ 5 mV,	R_S = 50 Ω			−0.3 to 4.2		V
V_{OH}	High-level output voltage	I_{OH} = −500 µA				4.88		V
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA			12		mV
		V_{IC} = 2.5 V,	I_{OL} = 500 µA			120		
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V	R_L = 2 kΩ†			5		V/mV
			R_L = 1 MΩ†			800		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	f = 10 kHz				6		pF
z_o	Closed-loop output impedance	f = 10 kHz,	A_V = 10			70		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V,	V_O = 0,	R_S = 50 Ω		85		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V,	V_{IC} = 0,	No load		95		dB
I_{DD}	Supply current	V_O = 0,		No load		110		µA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2721
INPUT OFFSET VOLTAGE**

545 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm1.5$ V
$T_A = 25°C$

Figure 1

**DISTRIBUTION OF TLV2721
INPUT OFFSET VOLTAGE**

545 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm2.5$ V
$T_A = 25°C$

Figure 2

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

$V_{DD} = 3$ V
$R_S = 50$ Ω
$T_A = 25°C$

Figure 3

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

$V_{DD} = 5$ V
$R_S = 50$ Ω
$T_A = 25°C$

Figure 4

† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2721 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

32 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 1.5$ V
P Package
$T_A = 25°C$ to $125°C$

α_{VIO} – Input Offset Voltage
Temperature Coefficient – μV/°C

Figure 5

DISTRIBUTION OF TLV2721 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT†

32 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 2.5$ V
P Package
$T_A = 25°C$ to $125°C$

α_{VIO} – Input Offset Voltage
Temperature Coefficient – μV/°C

Figure 6

INPUT BIAS AND INPUT OFFSET CURRENTS vs FREE-AIR TEMPERATURE

$V_{DD\pm} = \pm 2.5$ V
$V_{IC} = 0$
$V_O = 0$
$R_S = 50$ Ω

I_{IB}

I_{IO}

T_A – Free-Air Temperature – °C

Figure 7

INPUT VOLTAGE vs SUPPLY VOLTAGE

$R_S = 50$ Ω
$T_A = 25°C$

$|V_{IO}| \leq 5$ mV

$|V_{DD\pm}|$ – Supply Voltage – V

Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

INPUT VOLTAGE†‡
vs
FREE-AIR TEMPERATURE

Figure 9

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 10

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 11

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V$_{DD}$ = 5 V, all loads are referenced to 2.5 V. For all curves where V$_{DD}$ = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 13

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 14

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡
vs
FREQUENCY

Figure 15

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†‡
vs
FREE-AIR TEMPERATURE

Figure 17

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 18

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 19

DIFFERENTIAL VOLTAGE AMPLIFICATION‡
vs
LOAD RESISTANCE

Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE[†] AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN[†]
vs
FREQUENCY

Figure 22

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

$V_{DD} = 3$ V
$V_{IC} = 1.5$ V
$V_O = 0.5$ V to 2.5 V

$R_L = 1$ MΩ

$R_L = 2$ kΩ

A_{VD} – Large-Signal Differential Voltage Amplification – V/mV

T_A – Free-Air Temperature – °C

Figure 23

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE

$V_{DD} = 5$ V
$V_{IC} = 2.5$ V
$V_O = 1$ V to 4 V

$R_L = 1$ MΩ

$R_L = 2$ kΩ

A_{VD} – Large-Signal Differential Voltage Amplification – V/mV

T_A – Free-Air Temperature – °C

Figure 24

OUTPUT IMPEDANCE‡
vs
FREQUENCY

$V_{DD} = 3$ V
$T_A = 25$°C

$A_V = 100$

$A_V = 10$

$A_V = 1$

z_O – Output Impedance – Ω

f – Frequency – Hz

Figure 25

OUTPUT IMPEDANCE‡
vs
FREQUENCY

$V_{DD} = 5$ V
$T_A = 25$°C

$A_V = 100$

$A_V = 10$

$A_V = 1$

z_O – Output Impedance – Ω

f – Frequency – Hz

Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO†
vs
FREQUENCY

Figure 27

COMMON-MODE REJECTION RATIO†‡
vs
FREE-AIR TEMPERATURE

Figure 28

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREQUENCY

Figure 29

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREQUENCY

Figure 30

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO[†]
vs
FREE-AIR TEMPERATURE

V_{DD} = 2.7 V to 8 V
V_{IC} = V_O = V_{DD} /2

k_{SVR} – Supply-Voltage Rejection Ratio – dB

T_A – Free-Air Temperature – °C

Figure 31

SUPPLY CURRENT[†]
vs
SUPPLY VOLTAGE

V_O = 0
No Load

T_A = –40°C

T_A = 85°C

T_A = 25°C

I_{DD} – Supply Current – µA

V_{DD} – Supply Voltage – V

Figure 32

SLEW RATE[‡]
vs
LOAD CAPACITANCE

V_{DD} = 5 V
A_V = –1
T_A = 25°C

SR–

SR+

SR – Slew Rate – V/µs

C_L – Load Capacitance – pF

Figure 33

SLEW RATE[†][‡]
vs
FREE-AIR TEMPERATURE

V_{DD} = 5 V
R_L = 2 kΩ
C_L = 100 pF
A_V = 1

SR–

SR+

SR – Slew Rate – V/µs

T_A – Free-Air Temperature – °C

Figure 34

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
[‡] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE RESPONSE†

V_{DD} = 3 V
R_L = 2 kΩ
C_L = 100 pF
A_V = −1
T_A = 25°C

Figure 35

INVERTING LARGE-SIGNAL PULSE RESPONSE†

V_{DD} = 5 V
R_L = 2 kΩ
C_L = 100 pF
A_V = −1
T_A = 25°C

Figure 36

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

V_{DD} = 5 V
R_L = 2 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE†

V_{DD} = 5 V
C_L = 100 pF
A_V = 1
T_A = 25°C

R_L = 100 kΩ
Tied to 2.5 V

R_L = 2 kΩ
Tied to 2.5 V

R_L = 2 kΩ
Tied to 0 V

Figure 38

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL
PULSE RESPONSE†

V_{DD} = 3 V
R_L = 2 kΩ
C_L = 100 pF
A_V = −1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 39

INVERTING SMALL-SIGNAL
PULSE RESPONSE†

V_{DD} = 5 V
R_L = 2 kΩ
C_L = 100 pF
A_V = −1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 40

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

V_{DD} = 3 V
R_L = 2 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

V_{DD} = 5 V
R_L = 2 kΩ
C_L = 100 pF
A_V = 1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 42

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

Figure 43

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

Figure 44

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD†

Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY

Figure 46

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

Figure 47

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

Figure 48

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 49

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 51

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 52

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

Figure 53

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

Figure 54

APPLICATION INFORMATION

driving large capacitive loads

The TLV2721 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 50 through Figure 55 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins (R_{null} = 0).

A small series resistor (R_{null}) at the output of the device (Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 50 through Figure 53 show the effects of adding series resistances of 100 Ω, 200 Ω, 500 Ω, and 1 kΩ. The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \tag{1}$$

where :

$\Delta\phi_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (Figure 54 and Figure 55). To use equation 1, UGBW must be approximated from Figure 54 and Figure 55.
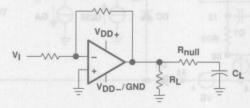
Figure 55. Series-Resistance Circuit

The TLV2721 is designed to provide better sinking and sourcing output currents than earlier CMOS rail-to-rail output devices. This device is specified to sink 500 µA and source 1 mA at V_{DD} = 5 V at a maximum quiescent I_{DD} of 200 µA. This provides a greater than 80% power efficiency.

When driving heavy dc loads, such as 2 kΩ, the positive edge under slewing conditions can experience some distortion. This condition can be seen in Figure 38. This condition is affected by three factors:

- Where the load is referenced. When the load is referenced to either rail, this condition does not occur. The distortion occurs only when the output signal swings through the point where the load is referenced. Figure 39 illustrates two 2-kΩ load conditions. The first load condition shows the distortion seen for a 2-kΩ load tied to 2.5 V. The third load condition in Figure 39 shows no distortion for a 2-kΩ load tied to 0 V.

- Load resistance. As the load resistance increases, the distortion seen on the output decreases. Figure 39 illustrates the difference seen on the output for a 2-kΩ load and a 100-kΩ load with both tied to 2.5 V.

- Input signal edge rate. Faster input edge rates for a step input result in more distortion than with slower input edge rates.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 57 are generated using the TLV2721 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).


```
.SUBCKT TLV2721 1 2 3 4 5
    C1      11   12    12.53E-12
    C2       6    7    50.00E-12
    DC       5   53    DX
    DE      54    5    DX
    DLP     90   91    DX
    DLN     92   90    DX
    DP       4    3    DX
    EGND    99    0    POLY (2) (3,0) (4,0) 0 .5 .5
    FB       7   99    POLY (5) VB VC VE VLP
    + VLN 0 893.6E3 –90E3 90E3 90E3 –90E3
    GA       6    0    11   12 94.25E–6
    GCM      0    6    10   99 9.300E–9
    ISS      3   10    DC 9.000E–6
    HLIM    90    0    VLIM 1K
    J1      11    2    10 JX
    J2      12    1    10 JX
    R2       6    9    100.0E3
```

```
    RD1     60   11    10.61E3
    RD2     60   12    10.61E3
    R01      8    5    35
    R02      7   99    35
    RP       3    4    49.50E3
    RSS     10   99    22.22E6
    VAD     60    4    –.5
    VB       9    0    DC 0
    VC      53    0    DC .666
    VE      54    4    DC .666
    VLIM     7    0    DC 0
    VLP     91    0    DC 3.4
    VLN      0   92    DC 11.4
.MODEL DX D (IS=800.0E–18)
.MODEL JX PJF (IS=500.0E–15 BETA=1.527E–3
+ VTO=–.001)
.ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

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TEXAS INSTRUMENTS

- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 15 nV/$\sqrt{Hz}$ Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Single-Supply 3-V and 5-V Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High Gain Bandwidth . . . 2 MHz at V_{DD} = 5 V with 600 Ω Load**
- **High Slew Rate . . . 1.6 V/µs at V_{DD} = 5 V**
- **Wide Supply Voltage Range 2.7 V to 10 V**
- **Macromodel Included**

DBV PACKAGE
(TOP VIEW)

```
OUT  | 1      5 |  V_DD- /GND
V_DD+| 2        |
IN+  | 3      4 |  IN-
```

description

The TLV2731 is a single low-voltage operational amplifier available in the SOT-23 package. It offers 2 MHz of bandwidth and 1.6 V/µs of slew rate for applications requiring good ac performance. The device exhibits rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV2731 is fully characterized at 3 V and 5 V and is optimized for low-voltage applications.

The TLV2731, exhibiting high input impedance and low noise, is excellent for small-signal conditioning of high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single- or split-supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). The device can also drive 600-Ω loads for telecom applications.

With a total area of 5.6mm², the SOT-23 package only requires one-third the board space of the standard 8-pin SOIC package. This ultra-small package allows designers to place single amplifiers very close to the signal source, minimizing noise pick-up from long PCB traces.

AVAILABLE OPTIONS
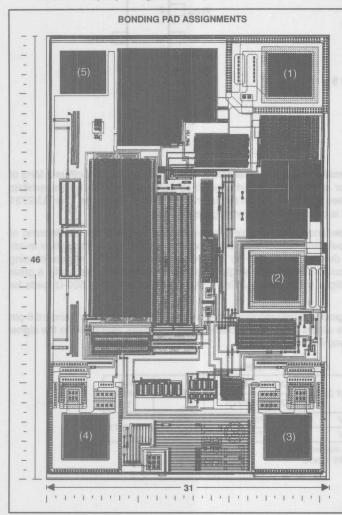
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES SOT-23 (DBV)†	SYMBOL	CHIP FORM‡ (Y)
0°C to 70°C	3 mV	TLV2731CDBV	VALC	TLV2731Y
−40°C to 85°C	3 mV	TLV2731IDBV	VALI	

† The DBV package available in tape and reel only.
‡ Chip forms are tested at T_A = 25°C only.

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TLV2731Y chip information

This chip, when properly assembled, displays characteristics similar to the TLV2731C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS

CHIP THICKNESS: 10 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (2) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic

COMPONENT COUNT†	
Transistors	23
Diodes	5
Resistors	11
Capacitors	2

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	12 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1)	-0.3 V to V_{DD}
Input current, I_I (each input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A: TLV2731C	0°C to 70°C
TLV2731I	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DBV package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25$°C POWER RATING	DERATING FACTOR ABOVE $T_A = 25$°C	$T_A = 70$°C POWER RATING	$T_A = 85$°C POWER RATING
DBV	150 mW	1.2 mW/°C	96 mW	78 mW

recommended operating conditions

	TLV2731C		TLV2731I		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD} (see Note 1)	2.7	10	2.7	10	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.3$	V_{DD-}	$V_{DD+} - 1.3$	V
Operating free-air temperature, T_A	0	70	-40	85	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

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electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2731C			TLV2731I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		0.7	3		0.7	3	mV
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD\pm} = \pm1.5$ V, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current		25°C		0.5			0.5		pA
			Full range			150			150	
I_{IB}	Input bias current		25°C		1			1		pA
			Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$, $|V_{IO}| \leq 5$ mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
			Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	25°C		2.87			2.87		V
		$I_{OH} = -2$ mA	25°C		2.74			2.74		
			Full range	2.3			2.3			
V_{OL}	Low-level output voltage	$V_{IC} = 1.5$ V, $I_{OL} = 50\ µA$	25°C		10			10		mV
		$V_{IC} = 1.5$ V, $I_{OL} = 500\ µA$	25°C		100			100		
			Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 1.5$ V, $V_O = 1$ V to 2 V, $R_L = 600\ \Omega$‡	25°C	1	1.6		1	1.6		V/mV
			Full range	0.3			0.3			
		$R_L = 1\ M\Omega$‡	25°C		250			250		
r_{id}	Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	$f = 10$ kHz	25°C		6			6		pF
z_O	Closed-loop output impedance	$f = 1$ MHz, $A_V = 1$	25°C		156			156		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 1.7 V, $V_O = 1.5$ V, $R_S = 50\ \Omega$	25°C	60	70		60	70		dB
			Full range	55			55			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} /\Delta V_{IO}$)	$V_{DD} = 2.7$ V to 8 V, $V_{IC} = V_{DD}/2$, No load	25°C	70	96		70	96		dB
			Full range	70			70			
I_{DD}	Supply current	$V_O = 1.5$ V, No load	25°C		750	1200		750	1200	µA
			Full range			1500			1500	

† Full range for the TLV2731C is 0°C to 70°C. Full range for the TLV2731I is − 40°C to 85°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2731C			TLV2731I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, R_L = 600 Ω‡, C_L = 100 pF‡		25°C	0.75	1.25		0.75	1.25		V/μs
				Full range	0.5			0.5			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		105			105		nV/√Hz
		f = 1 kHz		25°C		16			16		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.4			1.4		μV
		f = 0.1 Hz to 10 Hz		25°C		1.5			1.5		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	V_O = 1 V to 2 V, f = 20 kHz, R_L = 600 Ω‡	A_V = 1	25°C		0.285%			0.285%		
			A_V = 10			7.2%			7.2%		
		V_O = 1 V to 2 V, f = 20 kHz, R_L = 600 Ω§	A_V = 1	25°C		0.014%			0.014%		
			A_V = 10			0.098%			0.098%		
			A_V = 100			0.13%			0.13%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF‡	R_L = 600 Ω‡,	25°C		1.9			1.9		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 600 Ω‡,	A_V = 1, C_L = 100 pF‡	25°C		60			60		kHz
t_S	Settling time	A_V = –1, Step = 1 V to 2 V, R_L = 600 Ω‡, C_L = 100 pF‡	To 0.1%	25°C		0.9			0.9		μs
			To 0.01%			1.5			1.5		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω‡,	C_L = 100 pF‡	25°C		50°			50°		
	Gain margin			25°C		8			8		dB

† Full range is –40°C to 85°C.
‡ Referenced to 1.5 V
§ Referenced to 0 V

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2731C			TLV2731I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage			25°C		0.7	3		0.7	3	mV
α_{VIO}	Temperature coefficient of input offset voltage			Full range		0.5			0.5		µV/°C
	Input offset voltage long-term drift (see Note 4)	$V_{DD}\pm = \pm 2.5$ V, $V_O = 0$,	$V_{IC} = 0$, $R_S = 50$ Ω	25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5			0.5		pA
				Full range			150			150	
I_{IB}	Input bias current			25°C		1			1		pA
				Full range			150			150	
V_{ICR}	Common-mode input voltage range	$R_S = 50$ Ω,	$\|V_{IO}\| \le 5$ mV	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.7			0 to 3.7			
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA		25°C		4.9			4.9		V
		$I_{OH} = -4$ mA		25°C		4.6			4.6		
				Full range	4.3			4.3			
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 500$ µA	25°C		80			80		mV
		$V_{IC} = 2.5$ V,	$I_{OL} = 1$ mA	25°C		160			160		
				Full range			500			500	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V	$R_L = 600$ Ω‡	25°C	1	1.5		1	1.5		V/mV
				Full range	0.3			0.3			
			$R_L = 1$ MΩ‡	25°C		400			400		
r_{id}	Differential input resistance			25°C		10^{12}			10^{12}		Ω
r_{ic}	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
c_{ic}	Common-mode input capacitance	$f = 10$ kHz		25°C		6			6		pF
z_o	Closed-loop output impedance	$f = 1$ MHz,	$A_V = 1$	25°C		138			138		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 2.7 V, $V_O = 2.5$ V,	$R_S = 50$ Ω	25°C	60	70		60	70		dB
				Full range	55			55			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4$ V to 8 V, $V_{IC} = V_{DD}/2$,	No load	25°C	70	96		70	96		dB
				Full range	70			70			
I_{DD}	Supply current	$V_O = 2.5$ V,	No load	25°C		850	1300		850	1300	µA
				Full range			1600			1600	

† Full range for the TLV2731C is 0°C to 70°C. Full range for the TLV2731I is − 40°C to 85°C.
‡ Referenced to 2.5 V
NOTE 5: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

operating characteristics at specified free-air temperature, $V_{DD} = 5$ V

PARAMETER		TEST CONDITIONS		T_A†	TLV2731C			TLV2731I			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 1.5$ V to 3.5 V, $C_L = 100$ pF‡	$R_L = 600$ Ω‡,	25°C	1	1.6		1	1.6		V/μs
				Full range	0.7			0.7			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		100			100		nV/√Hz
		f = 1 kHz		25°C		15			15		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		1.4			1.4		μV
		f = 0.1 Hz to 10 Hz		25°C		1.5			1.5		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	$V_O = 1.5$ V to 3.5 V, f = 20 kHz, $R_L = 600$ Ω‡	$A_V = 1$	25°C		0.409%			0.409%		
			$A_V = 10$			3.68%			3.68%		
		$V_O = 1.5$ V to 3.5 V, f = 20 kHz, $R_L = 600$ Ω§	$A_V = 1$	25°C		0.018%			0.018%		
			$A_V = 10$			0.045%			0.045%		
			$A_V = 100$			0.116%			0.116%		
	Gain-bandwidth product	f = 10 kHz, $C_L = 100$ pF‡	$R_L = 600$ Ω‡,	25°C		2			2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 1$ V, $R_L = 600$ Ω‡,	$A_V = 1$, $C_L = 100$ pF‡	25°C		300			300		kHz
t_s	Settling time	$A_V = -1$, Step = 1.5 V to 3.5 V, $R_L = 600$ Ω‡, $C_L = 100$ pF‡	To 0.1%	25°C		0.95			0.95		μs
			To 0.01%			2.4			2.4		
$φ_m$	Phase margin at unity gain	$R_L = 600$ Ω‡,	$C_L = 100$ pF‡	25°C		48°			48°		
	Gain margin			25°C		8			8		dB

† Full range is –40°C to 85°C.
‡ Referenced to 2.5 V
§ Referenced to 0 V

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electrical characteristics at V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			TLV2731Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm = \pm1.5$ V,	$V_{IC} = 0$,	$V_O = 0$,		750		µV
I_{IO}	Input offset current	$R_S = 50\ \Omega$				0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq 5$ mV,	$R_S = 50\ \Omega$			−0.3 to 2.2		V
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA				2.87		V
V_{OL}	Low-level output voltage	$V_{IC} = 1.5$ V,	$I_{OL} = 50$ µA			10		mV
		$V_{IC} = 1.5$ V,	$I_{OL} = 500$ µA			100		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1$ V to 2 V	$R_L = 600\ \Omega$†			1.6		V/mV
			$R_L = 1$ MΩ†			250		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	$f = 10$ kHz				6		pF
z_o	Closed-loop output impedance	$f = 1$ MHz,	$A_V = 1$			156		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 1.7 V,	$V_O = 0$,	$R_S = 50\ \Omega$		70		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7$ V to 8 V,	$V_{IC} = 0$,	No load		96		dB
I_{DD}	Supply current	$V_O = 0$,	No load			750		µA

† Referenced to 1.5 V

electrical characteristics at V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			TLV2731Y			UNIT
					MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD}\pm = \pm1.5$ V,	$V_{IC} = 0$,	$V_O = 0$,		710		µV
I_{IO}	Input offset current	$R_S = 50\ \Omega$				0.5		pA
I_{IB}	Input bias current					1		pA
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \leq 5$ mV,	$R_S = 50\ \Omega$			−0.3 to 4.2		V
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA				4.9		V
V_{OL}	Low-level output voltage	$V_{IC} = 2.5$ V,	$I_{OL} = 500$ µA			80		mV
		$V_{IC} = 2.5$ V,	$I_{OL} = 1$ mA			160		
A_{VD}	Large-signal differential voltage amplification	$V_O = 1$ V to 2 V	$R_L = 600\ \Omega$†			15		V/mV
			$R_L = 1$ MΩ†			400		
r_{id}	Differential input resistance					10^{12}		Ω
r_{ic}	Common-mode input resistance					10^{12}		Ω
c_{ic}	Common-mode input capacitance	$f = 10$ kHz				6		pF
z_o	Closed-loop output impedance	$f = 1$ MHz,	$A_V = 1$			138		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ to 1.7 V,	$V_O = 0$,	$R_S = 50\ \Omega$		70		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 2.7$ V to 8 V,	$V_{IC} = 0$,	No load		96		dB
I_{DD}	Supply current	$V_O = 0$,	No load			850		µA

† Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

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		vs Free-air temperature	24, 25
z_o	Output impedance	vs Frequency	26, 27
CMRR	Common-mode rejection ratio	vs Frequency	28
		vs Free-air temperature	29
k_{SVR}	Supply-voltage rejection ratio	vs Frequency	30, 31
		vs Free-air temperature	32
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TEXAS INSTRUMENTS

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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2731
INPUT OFFSET VOLTAGE**

537 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 1.5\ V$
$T_A = 25°C$

Precentage of Amplifiers – %
V_{IO} – Input Offset Voltage – mV

Figure 1

**DISTRIBUTION OF TLV2731
INPUT OFFSET VOLTAGE**

537 Amplifiers From 1 Wafer Lot
$V_{DD} = \pm 2.5\ V$
$T_A = 25°C$

Precentage of Amplifiers – %
V_{IO} – Input Offset Voltage – mV

Figure 2

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

$V_{DD} = 3\ V$
$R_S = 50\ \Omega$
$T_A = 25°C$

V_{IO} – Input Offset Voltage – mV
V_{IC} – Common-Mode Input Voltage – V

Figure 3

**INPUT OFFSET VOLTAGE†
vs
COMMON-MODE INPUT VOLTAGE**

$V_{DD} = 5\ V$
$R_S = 50\ \Omega$
$T_A = 25°C$

V_{IO} – Input Offset Voltage – mV
V_{IC} – Common-Mode Input Voltage – V

Figure 4

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2731 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

32 Amplifiers From
1 Wafer Lots
$V_{DD\pm} = \pm 1.5$ V
P Package
$T_A = 25°C$ to $125°C$

α_{VIO} – Input Offset Voltage
Temperature Coefficient – μV/°C

Figure 5

DISTRIBUTION OF TLV2731 INPUT OFFSET
VOLTAGE TEMPERATURE COEFFICIENT†

32 Amplifiers From
1 Wafer Lots
$V_{DD\pm} = \pm 2.5$ V
P Package
$T_A = 25°C$ to $125°C$

α_{VIO} – Input Offset Voltage
Temperature Coefficient – μV/°C

Figure 6

INPUT BIAS AND INPUT OFFSET CURRENTS†
vs
FREE-AIR TEMPERATURE

$V_{DD\pm} = \pm 2.5$ V
$V_{IC} = 0$
$V_O = 0$
$R_S = 50$ Ω

I_{IB} I_{IO}

T_A – Free-Air Temperature – °C

Figure 7

INPUT VOLTAGE
vs
SUPPLY VOLTAGE

$R_S = 50$ Ω
$T_A = 25°C$

$|V_{IO}| \leq 5$ mV

$|V_{DD\pm}|$ – Supply Voltage – V

Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

Figure 9

HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 10

LOW-LEVEL OUTPUT VOLTAGE‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 11

LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT

Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS

**HIGH-LEVEL OUTPUT VOLTAGE†‡
vs
HIGH-LEVEL OUTPUT CURRENT**

Figure 13

**LOW-LEVEL OUTPUT VOLTAGE†‡
vs
LOW-LEVEL OUTPUT CURRENT**

Figure 14

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡
vs
FREQUENCY**

Figure 15

**SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE**

Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT†‡
vs
FREE-AIR TEMPERATURE

Figure 17

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 18

OUTPUT VOLTAGE‡
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 19

DIFFERENTIAL VOLTAGE AMPLIFICATION‡
vs
LOAD RESISTANCE

Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

V_{DD} = 3 V
R_L = 600 Ω
C_L = 100 pF
T_A = 25°C

Phase Margin

Gain

Figure 21

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

V_{DD} = 5 V
R_L = 600 Ω
C_L = 100 pF
T_A = 25°C

Phase Margin

Gain

Figure 22

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE**

Figure 23

**LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†‡
vs
FREE-AIR TEMPERATURE**

Figure 24

**OUTPUT IMPEDANCE‡
vs
FREQUENCY**

Figure 25

**OUTPUT IMPEDANCE‡
vs
FREQUENCY**

Figure 26

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO[†]
vs
FREQUENCY

Figure 27

COMMON-MODE REJECTION RATIO[†‡]
vs
FREE-AIR TEMPERATURE

Figure 28

SUPPLY-VOLTAGE REJECTION RATIO[†]
vs
FREQUENCY

Figure 29

SUPPLY-VOLTAGE REJECTION RATIO[†]
vs
FREQUENCY

Figure 30

[†] For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
[‡] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

SUPPLY-VOLTAGE REJECTION RATIO†
vs
FREE-AIR TEMPERATURE

Figure 31

SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

Figure 32

SLEW RATE‡
vs
LOAD CAPACITANCE

Figure 33

SLEW RATE†‡
vs
FREE-AIR TEMPERATURE

Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING LARGE-SIGNAL PULSE
RESPONSE†

V_{DD} = 3 V
R_L = 600 Ω
C_L = 100 pF
A_V = −1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 35

INVERTING LARGE-SIGNAL PULSE
RESPONSE†

V_{DD} = 5 V
R_L = 600 Ω
C_L = 100 pF
A_V = −1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 36

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE†

V_{DD} = 3 V
R_L = 600 Ω
C_L = 100 pF
A_V = 1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 37

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE†

V_{DD} = 5 V
R_L = 600 Ω
C_L = 100 pF
A_V = 1
T_A = 25°C

V_O – Output Voltage – V

t – Time – µs

Figure 38

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE†

$V_{DD} = 3 \text{ V}$
$R_L = 600 \text{ }\Omega$
$C_L = 100 \text{ pF}$
$A_V = -1$
$T_A = 25°C$

V_O – Output Voltage – V

t – Time – µs

Figure 39

INVERTING SMALL-SIGNAL PULSE RESPONSE†

$V_{DD} = 5 \text{ V}$
$R_L = 600 \text{ }\Omega$
$C_L = 100 \text{ pF}$
$A_V = -1$
$T_A = 25°C$

V_O – Output Voltage – V

t – Time – µs

Figure 40

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

$V_{DD} = 3 \text{ V}$
$R_L = 600 \text{ }\Omega$
$C_L = 100 \text{ pF}$
$A_V = 1$
$T_A = 25°C$

V_O – Output Voltage – V

t – Time – µs

Figure 41

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE†

$V_{DD} = 5 \text{ V}$
$R_L = 600 \text{ }\Omega$
$C_L = 100 \text{ pF}$
$A_V = 1$
$T_A = 25°C$

V_O – Output Voltage – V

t – Time – µs

Figure 42

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

$V_{DD} = 3\ V$
$R_S = 20\ \Omega$
$T_A = 25°C$

Figure 43

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

$V_{DD} = 5\ V$
$R_S = 20\ \Omega$
$T_A = 25°C$

Figure 44

INPUT NOISE VOLTAGE OVER
A 10-SECOND PERIOD†

$V_{DD} = 5\ V$
$f = 0.1\ Hz\ to\ 10\ Hz$
$T_A = 25°C$

Figure 45

TOTAL HARMONIC DISTORTION PLUS NOISE†
vs
FREQUENCY

$V_{DD} = 5\ V$
$T_A = 25°C$

$A_V = 10$
$A_V = 100$
$A_V = 1$
$A_V = 100$
$R_L = 600\ \Omega\ to\ 2.5\ V$
$R_L = 600\ \Omega\ to\ 0\ V$
$A_V = 10$
$A_V = 1$

Figure 46

† For all curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V. For all curves where $V_{DD} = 3$ V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT†‡
vs
FREE-AIR TEMPERATURE

V_{DD} = 5 V
f = 10 kHz
R_L = 600 Ω
C_L = 100 pF

T_A – Free-Air Temperature – °C

Figure 47

GAIN-BANDWIDTH PRODUCT‡
vs
SUPPLY VOLTAGE

R_L = 600 Ω
C_L = 100 pF
T_A = 25°C

V_{DD} – Supply Voltage – V

Figure 48

GAIN MARGIN‡
vs
LOAD CAPACITANCE

T_A = 25°
R_L = ∞

R_{null} = 100 Ω
R_{null} = 500 Ω
R_{null} = 1000 Ω
R_{null} = 50 Ω
R_{null} = 0

C_L – Load Capacitance – pF

Figure 49

GAIN MARGIN‡
vs
LOAD CAPACITANCE

T_A = 25°
R_L = 600 Ω

R_{null} = 100 Ω
R_{null} = 500 Ω
R_{null} = 50 Ω
R_{null} = 0

C_L – Load Capacitance – pF

Figure 50

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

PHASE MARGIN†
vs
LOAD CAPACITANCE

Figure 51

PHASE MARGIN†
vs
LOAD CAPACITANCE

Figure 52

UNITY-GAIN BANDWIDTH†
vs
LOAD CAPACITANCE

Figure 53

UNITY-GAIN BANDWIDTH†
vs
LOAD CAPACITANCE

Figure 54

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

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APPLICATION INFORMATION

driving large capacitive loads

The TLV2731 is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 50 through Figure 55 illustrate its ability to drive loads greater than 100 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A small series resistor (R_{null}) at the output of the device (see Figure 55) improves the gain and phase margins when driving large capacitive loads. Figure 50 through Figure 53 show the effects of adding series resistances of 50 Ω, 100 Ω, 500 Ω, and 1000 Ω. The addition of this series resistor has two effects: the first effect is that it adds a zero to the transfer function and the second effect is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the approximate improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1}\left(2 \times \pi \times UGBW \times R_{null} \times C_L\right)$$ (1)

where :

$\Delta\phi_{m1}$ = improvement in phase margin
$UGBW$ = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 54 and Figure 55). To use equation 1, UGBW must be approximated from Figure 54 and Figure 55.
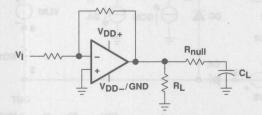
Figure 55. Series-Resistance Circuit

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 57 are generated using the TLV2731 typical electrical and operating characteristics at $T_A = 25°C$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).


```
.SUBCKT TLV2731 1 2 3 4 5
         C1      11    12    13.51E-12
         C2      6     7     50.00E-12
         DC      5     53    DX
         DE      54    5     DX
         DLP     90    91    DX
         DLN     92    90    DX
         DP      4     3     DX
         EGND    99    0     POLY (2) (3,0) (4,0) 0 .5 .5
         FB      7     99    POLY (5) VB VC VE VLP
       + VLN 0 90.83E3 –10E3 10E3 10E3 –10E3
         GA      6     0     11    12 314.2E–6
         GCM     0     6     10    99 242.35E–9
         ISS     3     10    DC    87.00E–6
         HLIM    90    0     VLIM 1K
         J1      11    2     10 JX
         J2      12    1     10 JX
         R2      6     9     100.0E3

         RD1     60    11    3.183E3
         RD2     60    12    3.183E3
         R01     8     5     25
         R02     7     99    25
         RP      3     4     6.553E3
         RSS     10    99    2.500E6
         VAD     60    4     –.5
         VB      9     0     DC 0
         VC      3     53    DC .795
         VE      54    4     DC .795
         VLIM    7     8     DC 0
         VLP     91    0     DC 12.4
         VLN     0     92    DC 17.4
         .MODEL DX D (IS=800.0E–18)
         .MODEL JX PJF (IS=500.0E–15 BETA=2.939E–3
       + VTO=–.065)
         .ENDS
```

Figure 56. Boyle Macromodel and Subcircuit

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- High Slew Rate . . . 10.5 V/μs Typ
- High-Gain Bandwidth . . . 5.1 MHz Typ
- Supply Voltage Range 2.5 V to 5.5 V
- Rail-to-Rail Output
- 360 μV Input Offset Voltage
- Low Distortion Driving 600-Ω 0.005% THD+N

- 1 mA Supply Current (Per Channel)
- 17 nV/√Hz Input Noise Voltage
- 2 pA Input Bias Current
- Characterized from T_A = −40°C to 125°C
- Available in MSOP and SOT-23 Packages
- Micropower Shutdown Mode . . . I_{DD} < 1 μA

description

The TLV277x CMOS operational amplifier family combines high slew rate and bandwidth, rail-to-rail output swing, high output drive, and excellent dc precision. The device provides 10.5 V/μs of slew rate and 5.1 MHz of bandwidth while only consuming 1 mA of supply current per channel. This ac performance is much higher than current competitive CMOS amplifiers. The rail-to-rail output swing and high output drive make these devices a good choice for driving the analog input or reference of analog-to-digital converters. These devices also have low distortion while driving a 600-Ω load for use in telecom systems.

These amplifiers have a 360 μV input offset voltage, a 17 nV/√Hz input noise voltage, and a 2 pA input bias current for measurement, medical, and industrial applications. The TLV277x family is also specified across an extended temperature range (−40°C to 125°C), making it useful for automotive systems.

These devices operate from a 2.5 V to 5.5 V single supply voltage and are characterized at 2.7 V and 5 V. The single-supply operation and low power consumption make these devices a good solution for portable applications. The following table lists the packages available.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES								SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	CDIP	SOIC	SOT-23	TSSOP	MSOP	LCCC	CPAK		
TLV2770	1	8	—	8	—	—	8	—	—	Yes	
TLV2771	1	—	—	8	5	—	—	—	—	—	
TLV2772	2	8	8	8	—	—	8	20	10	—	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2773	2	14	—	14	—	—	10	—	—	Yes	
TLV2774	4	14	—	14	—	14	—	—	—	—	
TLV2775	4	16	—	16	—	16	—	—	—	Yes	

A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS§

DEVICE	V_{DD} (V)	BW (MHz)	SLEW RATE (V/μs)	I_{DD} (per channel) (μA)	RAIL-TO-RAIL
TLV277X	2.5 – 6.0	5.1	10.5	1000	O
TLV247X	2.7 – 6.0	2.8	1.5	600	I/O
TLV245X	2.7 – 6.0	0.22	0.11	23	I/O
TLV246X	2.7 – 6.0	6.4	1.6	550	I/O

§ All specifications measured at 5 V.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

FAMILY OF 2.7-V HIGH-SLEW-RATE RAIL-TO-RAIL OUTPUT
OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS209D – JANUARY 1998 – REVISED NOVEMBER 1999

TLV2770 and TLV2771 AVAILABLE OPTIONS

T_A	V_IOmax AT 25°C (mV)	PACKAGED DEVICES			
		SMALL OUTLINE (D)	SOT-23 (DBV)	MSOP (DGK)	PLASTIC DIP (P)
0°C to 70°C	2.5	TLV2770CD TLV2771CD	— TLV2771CDBV	TLV2770CDGK† —	TLV2770CP —
−40°C to 125°C	2.5	TLV2770ID TLV2771ID	— TLV2771IDBV	TLV2770IDGK† —	TLV2770IP —
	1.6	TLV2770AID TLV2771AID	— —	— —	TLV2770AIP —

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

TLV2772 and TLV2773 AVAILABLE OPTIONS

T_A	V_IOmax AT 25°C (mV)	PACKAGED DEVICES				
		SMALL OUTLINE (D)	MSOP (DGK)	MSOP (DGS)	PLASTIC DIP (N)	PLASTIC DIP (P)
0°C to 70°C	2.5	TLV2772CD TLV2773CD	TLV2772CDGK —	— TLV2773CDGS	— TLV2773CN	TLV2772CP —
−40°C to 125°C	2.5	TLV2772ID TLV2773ID	TLV2772IDGK —	— TLV2773IDGS	— TLV2773IN	TLV2772IP —
	1.6	TLV2772AID TLV2773AID	— —	— —	— TLV2773AIN	TLV2772AIP —

TLV2774 and TLV2775 AVAILABLE OPTIONS

T_A	V_IOmax AT 25°C (mV)	PACKAGED DEVICES			
		SMALL OUTLINE (D)	PLASTIC DIP (N)	PLASTIC DIP (P)	TSSOP (PW)
0°C to 70°C	2.7	TLV2774CD TLV2775CD	— TLV2775CN	TLV2774CP —	TLV2774CPW TLV2775CPW
−40°C to 125°C	2.7	TLV2774ID TLV2775ID	— TLV2775IN	TLV2774IP —	TLV2774IPW TLV2775IPW
	2.1	TLV2774AID TLV2775AID	— TLV2775AIN	TLV2774AIP —	TLV2774AIPW TLV2775AIPW

TLV2772M AND TLV2772AM AVAILABLE OPTIONS

T_A	V_IOmax AT 25°C (mV)	PACKAGED DEVICES			
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	CERAMIC FLATPACK (U)
−55°C to 125°C	2.5	TLV2772MD	TLV2772MFK	TLV2772MJG	TLV2772MU
	1.6	TLV2772AMD	TLV2772AMFK	TLV2772AMJG	TLV2772AMU

![Texas Instruments logo] **TEXAS INSTRUMENTS**

PACKAGE SYMBOLS

PACKAGE TYPE	PINS	PART NUMBER	SYMBOL†
SOT23	5 Pin	TLV2771CDBV	VAMC
		TLV2771IDBV	VAMI
MSOP	8 Pin	TLV2770CDGK	xxTIABO
		TLV2770IDGK	xxTIABP
		TLV2772CDGK	xxTIAAF
		TLV2772IDGK	xxTIAAG
	10 Pin	TLV2773CDGS	xxTIABQ
		TLV2773IDGS	xxTIABR

† xx represents the device date code.

TLV277x PACKAGE PINOUTS

TLV2770
D, DGK† OR P PACKAGE
(TOP VIEW)

NC	1	8	SHDN
IN–	2	7	V_DD
IN+	3	6	OUT
GND	4	5	NC

TLV2771
DBV PACKAGE
(TOP VIEW)

OUT	1	5	V_DD
GND	2		
IN+	3	4	IN–

TLV2771
D PACKAGE
(TOP VIEW)

NC	1	8	NC
IN–	2	7	V_DD
IN+	3	6	OUT
GND	4	5	NC

TLV2772
D, DGK†, JG, OR P PACKAGE
(TOP VIEW)

1OUT	1	8	V_DD
1IN–	2	7	2OUT
1IN+	3	6	2IN–
GND	4	5	2IN+

TLV2772M AND TLV2772AM
U PACKAGE
(TOP VIEW)

NC	1	10	NC
1OUT	2	9	V_DD +
1IN –	3	8	2OUT
1IN +	4	7	2IN –
GND	5	6	2IN +

TLV2773
DGS PACKAGE
(TOP VIEW)

1OUT	1	10	V_DD
1IN–	2	9	2OUT
1IN+	3	8	2IN–
GND	4	7	2IN+
1SHDN	5	6	2SHDN

TLV2773
D OR N PACKAGE
(TOP VIEW)

1OUT	1	14	V_DD
1IN–	2	13	2OUT
1IN+	3	12	2IN–
GND	4	11	2IN+
NC	5	10	NC
1SHDN	6	9	2SHDN
NC	7	8	NC

TLV2774
D, N, OR PW PACKAGE
(TOP VIEW)

1OUT	1	14	4OUT
1IN–	2	13	4IN–
1IN+	3	12	4IN+
V_DD	4	11	GND
2IN+	5	10	3IN+
2IN–	6	9	3IN–
2OUT	7	8	3OUT

TLV2775
D, N, OR PW PACKAGE
(TOP VIEW)

1OUT	1	16	4OUT
1IN–	2	15	4IN–
1IN+	3	14	4IN+
V_DD	4	13	GND
2IN+	5	12	3IN+
2IN–	6	11	3IN–
2OUT	7	10	3OUT
1/2SHDN	8	9	3/4SHDN

TLV2772M AND TLV2772AM
FK PACKAGE
(TOP VIEW)

NC	4	18	NC
1IN–	5	17	2OUT
NC	6	16	NC
1IN+	7	15	2IN–
NC	8	14	NC

Top pins (3 2 1 20 19): NC, 1OUT, NC, V_DD+, NC
Bottom pins (9 10 11 12 13): NC, GND, NC, 2IN+, NC

NC – No internal connection

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 7 V
Differential input voltage, V_{ID} (see Note 2) .... $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) .... −0.3 V to V_{DD}
Input current, I_I (any input) .... ±4 mA
Output current, I_O .... ±50 mA
Total current into V_{DD+} .... ±50 mA
Total current out of GND .... ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) .... unlimited
Continuous total power dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix .... 0°C to 70°C
         I suffix .... −40°C to 125°C
         M suffix .... −55°C to 125°C
Storage temperature range, T_{stg} .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to GND.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below GND − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
DBV	437 mW	3.5 mW/°C	280 mW	227 mW	87 mW
DGK	424 mW	3.4 mW/°C	271 mW	220 mW	85 mW
DGS	424 mW	3.4 mW/°C	271 mW	220 mW	85 mW
FK	1375 mW	11.0 mW/°C	672 mW	546 mW	210 mW
JG	1050 mW	8.4 mW/°C	880 mW	714 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW
PW	700 mW	5.6 mW/°C	448 mW	364 mW	140 mW
U	675 mW	5.4 mW/°C	432 mW	350 mW	135 mW

recommended operating conditions

	C SUFFIX		I SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}	2.5	6	2.5	6	2.5	6	V
Input voltage range, V_I	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	V
Common-mode input voltage, V_{IC}	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	GND	$V_{DD+}-1.3$	V
Operating free-air temperature, T_A	0	70	−40	125	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV277xC MIN	TLV277xC TYP	TLV277xC MAX	UNIT
V_{IO} Input offset voltage	TLV2770/1/2	V_{IC} = 0, R_S = 50 Ω,	V_O = 0, V_{DD} = ±1.35 V	25°C		0.44	2.5	mV
				Full range		0.47	2.7	
	TLV2773/4/5			25°C		0.8	2.7	
				Full range		0.86	2.9	
α_{VIO} Temperature coefficient of input offset voltage				25°C to 125°C		2		μV/°C
I_{IO} Input offset current		V_{IC} = 0, R_S = 50 Ω	V_O = 0, V_{DD} = ±1.35 V	25°C		1		pA
				Full range		2	100	
I_{IB} Input bias current				25°C		2		pA
				Full range		6	100	
V_{ICR} Common-mode input voltage range		CMRR > 70 dB,	R_S = 50 Ω	25°C	0 to 1.4	−0.3 to 1.7		V
				Full range	0 to 1.4	−0.3 to 1.7		
V_{OH} High-level output voltage		I_{OH} = −0.675 mA		25°C		2.6		V
				Full range	2.5			
		I_{OH} = −2.2 mA		25°C		2.4		
				Full range	2.1			
V_{OL} Low-level output voltage		V_{IC} = 1.35 V,	I_{OL} = 0.675 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 1.35 V,	I_{OL} = 2.2 mA	25°C		0.21		
				Full range			0.6	
A_{VD} Large-signal differential voltage amplification		V_{IC} = 1.35 V, V_O = 0.6 V to 2.1 V	R_L = 10 kΩ,	25°C	20	380		V/mV
				Full range	13			
$r_{i(d)}$ Differential input resistance				25°C		10^{12}		Ω
$c_{i(c)}$ Common-mode input capacitance		f = 10 kHz		25°C		8		pF
z_O Closed-loop output impedance		f = 100 kHz,	A_V = 10	25°C		25		Ω
CMRR Common-mode rejection ratio		V_{IC} = 0 to 1.5 V, R_S = 50 Ω	V_O = 1.5 V,	25°C	70	84		dB
				Full range	70	82		
k_{SVR} Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		dB
				Full range	70	84		
I_{DD} Supply current (per channel)		V_O = 1.5 V,	No load	25°C		1	2	mA
				Full range			2	
$I_{DD(SHDN)}$ Supply current in shutdown (per channel)				25°C		0.8	1.5	μA
				Full range		1.3	2	
$V_{(ON)}$ Turnon voltage level	TLV2770	A_V = 5		25°C		1.47		V
	TLV2773					1.43		
	TLV2775					1.40		
$V_{(OFF)}$ Turnoff voltage level	TLV2770	A_V = 5		25°C		1.27		V
	TLV2773					1.21		
	TLV2775					1.20		

† Full range is 0°C to 70°C.

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operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV277xC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 100 pF,	25°C	5	9		V/µs
				Full range	4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21		nV/√Hz
		f = 10 kHz		25°C		17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33		µV
		f = 0.1 Hz to 10 Hz				0.86		
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%		
			A_V = 10			0.025%		
			A_V = 100			0.12%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		4.8		MHz
t_S	Settling time	A_V = −1, Step = 1 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186		µs
			0.01%	25°C		0.3		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω,	C_L = 100 pF	25°C		46°		
	Gain margin			25°C		12		dB

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV277xC MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	TLV2770/1/2	V_{IC} = 0, R_S = 50 Ω	V_O = 0, V_{DD} = ±2.5 V	25°C		0.36	2.5	mV
				Full range		0.4	2.7	
	TLV2773/4/5			25°C		0.7	2.5	
				Full range		0.78	2.7	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2		µV/°C
I_{IO}	Input offset current	V_{IC} = 0, R_S = 50 Ω	V_O = 0, V_{DD} = ±2.5 V	25°C		1		pA
				Full range		2	100	
I_{IB}	Input bias current			25°C		2		pA
				Full range		6	100	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB,	R_S = 50 Ω	25°C	0 to 3.7	−0.3 to 3.8		V
				Full range	0 to 3.7	−0.3 to 3.8		
V_{OH}	High-level output voltage	I_{OH} = −1.3 mA		25°C		4.9		V
				Full range	4.8			
		I_{OH} = −4.2 mA		25°C		4.7		
				Full range	4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 1.3 mA	25°C		0.1		V
				Full range			0.2	
		V_{IC} = 2.5 V,	I_{OL} = 4.2 mA	25°C		0.21		
				Full range			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 10 kΩ,	25°C	20	450		V/mV
				Full range	13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz		25°C		8		pF
z_O	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3.7 V, R_S = 50 Ω	V_O = 3.7 V,	25°C	60	96		dB
				Full range	60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	70	89		dB
				Full range	70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V,	No load	25°C		1	2	mA
				Full range			2	
$I_{DD(SHDN)}$	Supply current in shutdown (per channel)			25°C		0.8	1.5	µA
				Full range		1.3	2	
$V_{(ON)}$	Turnon voltage level	TLV2770	A_V = 5	25°C		2.59		V
		TLV2773				2.47		
		TLV2775				2.48		
$V_{(OFF)}$	Turnoff voltage level	TLV2770	A_V = 5	25°C		2.41		V
		TLV2773				2.32		
		TLV2775				2.29		

† Full range is 0°C to 70°C.

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operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		T_A†	TLV277xC			UNIT
						MIN	TYP	MAX	
SR	Slew rate at unity gain		$V_{O(PP)}$ = 1.5 V, R_L = 10 kΩ	C_L = 100 pF,	25°C	5	10.5		V/µs
					Full range	4.7	6		
V_n	Equivalent input noise voltage		f = 1 kHz		25°C		17		nV/√Hz
			f = 10 kHz		25°C		12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage		f = 0.1 Hz to 1 Hz		25°C		0.33		µV
			f = 0.1 Hz to 10 Hz				0.86		
I_n	Equivalent input noise current		f = 100 Hz		25°C		0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise		R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%		
				A_V = 10			0.016%		
				A_V = 100			0.095%		
	Gain-bandwidth product		f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		5.1		MHz
t_S	Settling time		A_V = −1, Step = 2 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.335		µs
				0.01%	25°C		0.6		
ϕ_m	Phase margin at unity gain		R_L = 600 Ω,	C_L = 100 pF	25°C		46°		
	Gain margin				25°C		12		dB
$t_{(ON)}$	Amplifier turnon time	TLV2770	A_V = 5, R_L = Open, Measured to 50% point		25°C		1.2		µs
		TLV2773					2.4		
		TLV2775					1.9		
$t_{(OFF)}$	Amplifier turnoff time	TLV2770	A_V = 5 R_L = Open, Measured to 50% point		25°C		335		ns
		TLV2773					444		
		TLV2775					345		

† Full range is 0°C to 70°C.

electrical characteristics at specified free-air temperature, $V_{DD} = 2.7$ V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLV2770/1/2	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\,\Omega$ $V_{DD} = \pm1.35$ V	25°C		0.44	2.5		0.44	1.6	mV
				Full range		0.47	2.7		0.47	1.9	
		TLV2773/4/5		25°C		0.8	2.7		0.8	2.1	
				Full range		0.86	2.9		0.86	2.2	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current		$V_{IC} = 0$, $V_O = 0$, $R_S = 50\,\Omega$	25°C		1			1		pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2			2		pA
				Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range		CMRR > 70 dB, $R_S = 50\,\Omega$	25°C	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		V
				Full range	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		
V_{OH}	High-level output voltage		$I_{OH} = −0.675$ mA	25°C		2.6			2.6		V
				Full range	2.5			2.5			
			$I_{OH} = −2.2$ mA	25°C		2.4			2.4		
				Full range	2.1			2.1			
V_{OL}	Low-level output voltage		$V_{IC} = 1.35$ V, $I_{OL} = 0.675$ mA	25°C		0.1			0.1		V
				Full range			0.2			0.2	
			$V_{IC} = 1.35$ V, $I_{OL} = 2.2$ mA	25°C		0.21			0.21		
				Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification		$V_{IC} = 1.35$ V, $R_L = 10$ kΩ, $V_O = 0.6$ V to 2.1 V	25°C	20	380		20	380		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance		f = 10 kHz,	25°C		8			8		pF
z_o	Closed-loop output impedance		f = 100 kHz, $A_V = 10$	25°C		25			25		Ω
CMRR	Common-mode rejection ratio		$V_{IC} = 0$ to 1.5 V, $V_O = 1.5$ V, $R_S = 50\,\Omega$	25°C	70	84		70	84		dB
				Full range	70	82		70	82		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		$V_{DD} = 2.7$ V to 5 V, $V_{IC} = V_{DD}/2$, No load	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)		$V_O = 1.5$ V, No load	25°C		1	2		1	2	mA
				Full range			2			2	
$I_{DD(SHDN)}$	Supply current in shutdown (per channel)			25°C		0.8	1.5		0.8	1.5	µA
				Full range		1.3	2		1.3	2	

† Full range is − 40°C to 125°C.

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electrical characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(ON)}$	Turnon voltage level	TLV2770	$A_V = 5$	25°C		1.47			1.47		V
		TLV2773				1.43			1.43		
		TLV2775				1.40			1.4		
$V_{(OFF)}$	Turnoff voltage level	TLV2770	$A_V = 5$	25°C		1.27			1.27		V
		TLV2773				1.21			1.21		
		TLV2775				1.20			1.2		

† Full range is – 40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	9		5	9		V/µs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21			21		nV/√Hz
		f = 10 kHz		25°C		17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	$A_V = 1$	25°C		0.0085%			0.0085%		
			$A_V = 10$			0.025%			0.025%		
			$A_V = 100$			0.12%			0.12%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		4.8			4.8		MHz
t_s	Settling time	$A_V = -1$, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186			0.186		µs
			0.01%	25°C		3.92			3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is −40°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLV2770/1/2	V_{IC} = 0, V_O = 0, R_S = 50 Ω, V_{DD} = ±2.5 V	25°C		0.36	2.5		0.36	1.6	mV
				Full range		0.4	2.7		0.4	1.9	
		TLV2773/4/5		25°C		0.7	2.5		0.7	2.1	
				Full range		0.78	2.7		0.78	2.2	
α_{VIO}	Temperature coefficient of input offset voltage		V_{IC} = 0, V_O = 0, R_S = 50 Ω, V_{DD} = ±2.5 V	25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current			25°C		1			1		pA
				Full range		2	125		2	125	
I_{IB}	Input bias current			25°C		2			2		pA
				Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range		CMRR > 60 dB, R_S = 50 Ω	25°C	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		V
				Full range	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		
V_{OH}	High-level output voltage		I_{OH} = −1.3 mA	25°C		4.9			4.9		V
				Full range	4.8			4.8			
			I_{OH} = −4.2 mA	25°C		4.7			4.7		
				Full range	4.4			4.4			
V_{OL}	Low-level output voltage		V_{IC} = 2.5 V, I_{OL} = 1.3 mA	25°C		0.1			0.1		V
				Full range			0.2			0.2	
			V_{IC} = 2.5 V, I_{OL} = 4.2 mA	25°C		0.21			0.21		
				Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification		V_{IC} = 2.5 V, R_L = 10 kΩ, V_O = 1 V to 4 V	25°C	20	450		20	450		V/mV
				Full range	13			13			
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance		f = 10 kHz	25°C		8			8		pF
z_o	Closed-loop output impedance		f = 100 kHz, A_V = 10	25°C		20			20		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 3.7 V, V_O = 3.7 V, R_S = 50 Ω	25°C	60	96		60	96		dB
				Full range	60	93		60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 5 V, V_{IC} = V_{DD}/2, No load	25°C	70	89		70	89		dB
				Full range	70	84		70	84		
I_{DD}	Supply current (per channel)		V_O = 1.5 V, No load	25°C		1	2		1	2	mA
				Full range			2			2	
$I_{DD(SHDN)}$	Supply current shutdown (per channel)			25°C		0.8	1.5		0.8	1.5	µA
				Full range		1.3	2		1.3	2	

† Full range is − 40°C to 125°C.

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electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV277xI			TLV277xAI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{(ON)}$	Turnon voltage level	TLV2770	A_V = 5	25°C		2.59			2.59		V
		TLV2773				2.47			2.47		
		TLV2775				2.48			2.48		
$V_{(OFF)}$	Turnoff voltage level	TLV2770	A_V = 5	25°C		2.41			2.41		V
		TLV2773				2.32			2.32		
		TLV2775				2.29			2.29		

† Full range is – 40°C to 125°C.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV277xI			TLV277xAI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		5	10.5		V/μs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		17			17		nV/√Hz
		f = 10 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		μV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		μV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%			0.005%		
			A_V = 10			0.016%			0.016%		
			A_V = 100			0.095%			0.095%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		5.1			5.1		MHz
t_s	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134			0.134		μs
			0.01%	25°C		1.97			1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB
$t_{(ON)}$	Amplifier turnon time	TLV2770	A_V = 5, R_L = Open, Measured to 50% point	25°C		1.2			1.2		μs
		TLV2773				2.4			2.4		
		TLV2775				1.9			1.9		
$t_{(OFF)}$	Amplifier turnoff time	TLV2770	A_V = 5, R_L = Open, Measured to 50% point	25°C		335			335		ns
		TLV2773				444			444		
		TLV2775				345			345		

† Full range is –40°C to 125°C.

electrical characteristics at specified free-air temperature, $V_{DD} = 2.7$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A[†]	TLV2772M			TLV2772AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage		25°C		0.44	2.5		0.44	1.6	mV
			Full range		0.47	2.7		0.47	1.9	
α_{VIO}	Temperature coefficient of input offset voltage	$V_{DD} = \pm1.35$ V, $V_{IC} = 0$, $R_S = 50\ \Omega$	25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current		25°C		1			1		pA
		$V_O = 0$,	Full range		2	125		2	125	
I_{IB}	Input bias current		25°C		2			2		pA
			Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range	CMRR > 70 dB, $R_S = 50\ \Omega$	25°C	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		V
			Full range	0 to 1.4	−0.3 to 1.7		0 to 1.4	−0.3 to 1.7		
V_{OH}	High-level output voltage	$I_{OH} = -0.675$ mA	25°C		2.6			2.6		V
			Full range	2.45			2.45			
		$I_{OH} = -2.2$ mA	25°C		2.4			2.4		
			Full range	2.1			2.1			
V_{OL}	Low-level output voltage	$V_{IC} = 1.35$ V, $I_{OL} = 0.675$ mA	25°C		0.1			0.1		V
			Full range			0.2			0.2	
		$V_{IC} = 1.35$ V, $I_{OL} = 2.2$ mA	25°C		0.21			0.21		
			Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	$V_{IC} = 1.35$ V, $R_L = 10\ k\Omega$,[‡] $V_O = 0.6$ V to 2.1 V	25°C	20	380		20	380		V/mV
			Full range	13			13			
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	$f = 10$ kHz,	25°C		8			8		pF
z_O	Closed-loop output impedance	$f = 100$ kHz, $A_V = 10$	25°C		25			25		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$ (min), $V_O = 1.5$ V, $R_S = 50\ \Omega$	25°C	70	84		70	84		dB
			Full range	70	82		70	82		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	$V_{DD} = 2.7$ V to 5 V, $V_{IC} = V_{DD}/2$, No load	25°C	70	89		70	89		dB
			Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	$V_O = 1.5$ V, No load	25°C		1	2		1	2	mA
			Full range			2			2	

† Full range is − 55°C to 125°C.
‡ Referenced to 1.35 V

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operating characteristics at specified free-air temperature, V_{DD} = 2.7 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		T_A†	TLV2772M			TLV2772AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	9		5	9		V/μs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		21			21		nV/√Hz
		f = 10 kHz		25°C		17			17		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		μV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		μV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.0085%			0.0085%		
			A_V = 10			0.025%			0.025%		
			A_V = 100			0.12%			0.12%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		4.8			4.8		MHz
t_S	Settling time	A_V = −1, Step = 0.85 V to 1.85 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.186			0.186		μs
			0.01%	25°C		3.92			3.92		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is −55°C to 125°C.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	TLV2772M MIN	TYP	MAX	TLV2772AM MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		0.36	2.5		0.36	1.6	mV
			Full range		0.4	2.7		0.4	1.9	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω	25°C to 125°C		2			2		µV/°C
I_{IO}	Input offset current		25°C		1			1		pA
			Full range		2	125		2	125	
I_{IB}	Input bias current		25°C		2			2		pA
			Full range		6	350		6	350	
V_{ICR}	Common-mode input voltage range	CMRR > 60 dB, R_S = 50 Ω	25°C	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		V
			Full range	0 to 3.7	−0.3 to 3.8		0 to 3.7	−0.3 to 3.8		
V_{OH}	High-level output voltage	I_{OH} = −1.3 mA	25°C		4.9			4.9		V
			Full range	4.8			4.8			
		I_{OH} = −4.2 mA	25°C		4.7			4.7		
			Full range	4.4			4.4			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OL} = 1.3 mA	25°C		0.1			0.1		V
			Full range			0.2			0.2	
		V_{IC} = 2.5 V, I_{OL} = 4.2 mA	25°C		0.21			0.21		
			Full range			0.6			0.6	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V, R_L = 10 kΩ,‡	25°C	20	450		20	450		V/mV
			Full range	13			13			
$r_{i(d)}$	Differential input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz, A_V = 10	25°C		20			20		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} (min), V_O = 3.7 V, R_S = 50 Ω	25°C	60	96		60	96		dB
			Full range	60	93		60	93		
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})	V_{DD} = 2.7 V to 5 V, No load, V_{IC} = V_{DD}/2,	25°C	70	89		70	89		dB
			Full range	70	84		70	84		
I_{DD}	Supply current (per channel)	V_O = 1.5 V, No load	25°C		1	2		1	2	mA
			Full range			2			2	

† Full range is − 55°C to 125°C.
‡ Referenced to 2.5 V

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2772M			TLV2772AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_{O(PP)}$ = 1.5 V, C_L = 100 pF, R_L = 10 kΩ		25°C	5	10.5		5	10.5		V/µs
				Full range	4.7	6		4.7	6		
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		17			17		nV/√Hz
		f = 10 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.33			0.33		µV
		f = 0.1 Hz to 10 Hz		25°C		0.86			0.86		µV
I_n	Equivalent input noise current	f = 100 Hz		25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	R_L = 600 Ω, f = 1 kHz	A_V = 1	25°C		0.005%			0.005%		
			A_V = 10			0.016%			0.016%		
			A_V = 100			0.095%			0.095%		
	Gain-bandwidth product	f = 10 kHz, C_L = 100 pF	R_L = 600 Ω,	25°C		5.1			5.1		MHz
t_S	Settling time	A_V = –1, Step = 1.5 V to 3.5 V, R_L = 600 Ω, C_L = 100 pF	0.1%	25°C		0.134			0.134		µs
			0.01%	25°C		1.97			1.97		
ϕ_m	Phase margin at unity gain	R_L = 600 Ω, C_L = 100 pF		25°C		46°			46°		
	Gain margin			25°C		12			12		dB

† Full range is –55°C to 125°C.

TYPICAL CHARACTERISTICS

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		vs Free-air temperature	25
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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE**

V_{DD} = 2.7 V
R_L = 10 kΩ
T_A = 25°C

Percentage of Amplifiers – %

V_{IO} – Input Offset Voltage – mV

Figure 1

**DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE**

V_{DD} = 5 V
R_L = 10 kΩ
T_A = 25°C

Percentage of Amplifiers – %

V_{IO} – Input Offset Voltage – mV

Figure 2

**INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

V_{DD} = 2.7 V
T_A = 25°C

V_{IO} – Input Offset Voltage – mV

V_{IC} – Common-Mode Input Voltage – V

Figure 3

**INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE**

V_{DD} = 5 V
T_A = 25°C

V_{IO} – Input Offset Voltage – mV

V_{IC} – Common-Mode Input Voltage – V

Figure 4

**TEXAS
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TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE**

Figure 5

**DISTRIBUTION OF TLV2772
INPUT OFFSET VOLTAGE**

Figure 6

**INPUT BIAS AND OFFSET CURRENT
vs
FREE-AIR TEMPERATURE**

Figure 7

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT**

Figure 8

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 11

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 12

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TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

Figure 13

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

Figure 14

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

Figure 15

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 16

TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE MARGIN
vs
FREQUENCY**

Figure 17

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE MARGIN
vs
FREQUENCY**

Figure 18

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TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

Figure 19

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 20

DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

Figure 21

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 22

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TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE
vs
FREQUENCY

Figure 23

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

Figure 24

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

Figure 25

SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 26

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TYPICAL CHARACTERISTICS

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

Figure 27

SUPPLY CURRENT (PER CHANNEL)
vs
SUPPLY VOLTAGE

Figure 28

SLEW RATE
vs
LOAD CAPACITANCE

Figure 29

SLEW RATE
vs
FREE-AIR TEMPERATURE

Figure 30

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TYPICAL CHARACTERISTICS

**VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE**

Figure 31

**VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE**

Figure 32

**VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE**

Figure 33

**VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE**

Figure 34

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL
PULSE RESPONSE

V_{DD} = 2.7 V
R_L = 600 Ω
C_L = 100 pF
AV = –1
T_A = 25°C

Figure 35

INVERTING SMALL-SIGNAL
PULSE RESPONSE

V_{DD} = 5 V
R_L = 600 Ω
C_L = 100 pF
AV = –1
T_A = 25°C

Figure 36

INVERTING LARGE-SIGNAL
PULSE RESPONSE

V_{DD} = 2.7 V
R_L = 600 Ω
C_L = 100 pF
AV = –1
T_A = 25°C

Figure 37

INVERTING LARGE-SIGNAL
PULSE RESPONSE

V_{DD} = 5 V
R_L = 600 Ω
C_L = 100 pF
AV = –1
T_A = 25°C

Figure 38

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TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

$V_{DD} = 2.7 \text{ V}$
$R_S = 20 \ \Omega$
$T_A = 25°C$

Figure 39

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

$V_{DD} = 5 \text{ V}$
$R_S = 20 \ \Omega$
$T_A = 25°C$

Figure 40

NOISE VOLTAGE
OVER A 10 SECOND PERIOD

$V_{DD} = 5 \text{ V}$
$f = 0.1 \text{ Hz to } 10 \text{ Hz}$
$T_A = 25°C$

Figure 41

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 42

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 43

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

Figure 44

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

Figure 45

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TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
LOAD CAPACITANCE

Figure 46

GAIN MARGIN
vs
LOAD CAPACITANCE

Figure 47

TYPICAL CHARACTERISTICS

TLV2770
AMPLIFIER WITH A SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

Figure 48

TLV2773
AMPLIFIER WITH A SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

Figure 49

TLV2775 – CHANNEL 1
AMPLIFIER WITH A SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

Figure 50

TLV2770
SUPPLY CURRENT WITH A SHUTDOWN PULSE
TURNON/OFF CHARACTERISTICS

Figure 51

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TYPICAL CHARACTERISTICS

TLV2773
SUPPLY CURRENT WITH A SHUTDOWN PULSE TURNON/OFF CHARACTERISTICS

$\overline{SHDN} = V_{DD}$

$\overline{SHDN} = GND$

$V_{DD} = 5$ V
$A_V = 5$
$T_A = 25°C$
Channel 1 Switched
Channel 2 $\overline{SHDN}$ MODE

I_{DD}

Shutdown Signal – V

I_{DD} – Supply Current – mA

t – Time – μs

Figure 52

TLV2775
SUPPLY CURRENT WITH A SHUTDOWN PULSE TURNON/OFF CHARACTERISTICS

$\overline{SHDN} = V_{DD}$

$\overline{SHDN} = GND$

$V_{DD} = 5$ V
$A_V = 5$
$T_A = 25°C$
Channel 1/2 Switched
Channel 3/4 $\overline{SHDN}$ MODE

I_{DD}

Shutdown Signal – V

I_{DD} – Supply Current – mA

t – Time – μs

Figure 53

SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE

$A_V = 5$
$R_L = OPEN$
$\overline{SHDN} = GND$

V_{DD} 5 V

V_{DD} 2.7 V

I_{DD} – Supply Current – μA

T_A – Free-Air Temperature – °C

Figure 54

TLV2770
SHUTDOWN FORWARD ISOLATION vs FREQUENCY

$V_{I(PP)} = 2.7$ V

$V_{I(PP)} = 0.1$ V

SHDN MODE
$A_V = 1$
$V_{DD} = 2.7$ V
$R_L = 10$ kΩ
$C_L = 20$ pF
$T_A = 25°C$

Forward Isolation – dB

f – Frequency – Hz

Figure 55

TYPICAL CHARACTERISTICS

TLV2770
SHUTDOWN REVERSE ISOLATION
vs
FREQUENCY

Figure 56

PARAMETER MEASUREMENT INFORMATION

Figure 57

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APPLICATION INFORMATION

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 58. A minimum value of 20 Ω should work well for most applications.
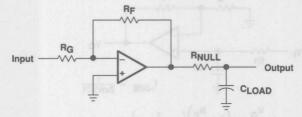
Figure 58. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+} \; R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} \; R_F$$
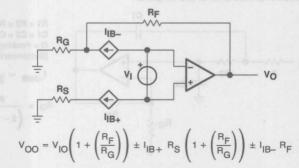
Figure 59. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 60).

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$
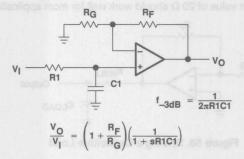
Figure 60. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$
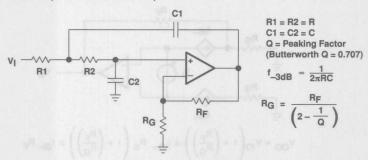
Figure 61. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

using the TLV2772 as an accelerometer interface

The schematic, shown in Figure 62, shows the ACH04-08-05 interfaced to the TLV1544 10-bit analog-to-digital converter (ADC).

The ACH04-08-05 is a shock sensor designed to convert mechanical acceleration into electrical signals. The sensor contains three piezoelectric sensing elements oriented to simultaneously measure acceleration in three orthogonal, linear axes (x, y, z). The operating frequency is 0.5 Hz to 5 kHz. The output is buffered with an internal JFET and has a typical output voltage of 1.80 mV/g for the x and y axis and 1.35 mV/g for the z axis.

Amplification and frequency shaping of the shock sensor output is done by the TLV2772 rail-to-rail operational amplifier. The TLV2772 is ideal for this application as it offers high input impedance, good slew rate, and excellent dc precision. The rail-to-rail output swing and high output drive are perfect for driving the analog input of the TLV1544 ADC.
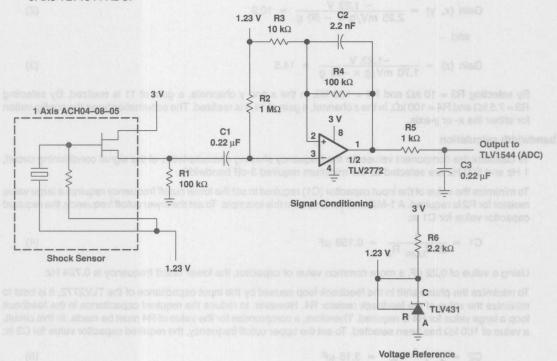
Figure 62. Accelerometer Interface Schematic

The sensor signal must be amplified and frequency-shaped to provide a signal the ADC can properly convert into the digital domain. Figure 62 shows the topology used in this application for one axis of the sensor. This system is powered from a single 3-V supply. Configuring the TLV431 with a 2.2-kΩ resistor produces a reference voltage of 1.23 V. This voltage is used to bias the operational amplifier and the internal JFETs in the shock sensor.

APPLICATION INFORMATION

gain calculation

Since the TLV2772 is capable of rail-to-rail output using a 3-V supply, $V_O = 0$ (min) to 3 V (max). With no signal from the sensor, nominal V_O = reference voltage = 1.23 V. Therefore, the maximum negative swing from nominal is $0 V - 1.23 V = -1.23$ V and the maximum positive swing is $3 V - 1.23 V = 1.77$ V. By modeling the shock sensor as a low impedance voltage source with output of 2.25 mV/g (max) in the x and y axis and 1.70 mV/g (max) in the z axis, the gain of the circuit is calculated by equation 1.

$$\text{Gain} = \frac{\text{Output Swing}}{\text{Sensor Signal} \times \text{Acceleration}} \tag{1}$$

To avoid saturation of the operational amplifier, the gain calculations are based on the maximum negative swing of –1.23 V and the maximum sensor output of 2.25 mV/g (x and y axis) and 1.70 mV/g (z axis).

$$\text{Gain (x, y)} = \frac{-1.23 \text{ V}}{2.25 \text{ mV/g} \times -50 \text{ g}} = 10.9 \tag{2}$$

and

$$\text{Gain (z)} = \frac{-1.23 \text{ V}}{1.70 \text{ mV/g} \times -50 \text{ g}} = 14.5 \tag{3}$$

$$(2)$$

By selecting R3 = 10 kΩ and R4 = 100 kΩ, in the x and y channels, a gain of 11 is realized. By selecting R3 = 7.5 kΩ and R4 = 100 kΩ, in the z channel, a gain of 14.3 is realized. The schematic shows the configuration for either the x- or y-axis.

bandwidth calculation

To calculate the component values for the frequency shaping characteristics of the signal conditioning circuit, 1 Hz and 500 Hz are selected as the minimum required 3-dB bandwidth.

To minimize the value of the input capacitor (C1) required to set the lower cutoff frequency requires a large value resistor for R2 is required. A 1-MΩ resistor is used in this example. To set the lower cutoff frequency, the required capacitor value for C1 is:

$$C1 = \frac{1}{2\pi \, f_{LOW} \, R_2} = 0.159 \, \mu F \tag{4}$$

Using a value of 0.22 µF, a more common value of capacitor, the lower cutoff frequency is 0.724 Hz.

To minimize the phase shift in the feedback loop caused by the input capacitance of the TLV2772, it is best to minimize the value of the feedback resistor R4. However, to reduce the required capacitance in the feedback loop a large value for R4 is required. Therefore, a compromise for the value of R4 must be made. In this circuit, a value of 100 kΩ has been selected. To set the upper cutoff frequency, the required capacitor value for C2 is:

$$C2 = \frac{1}{2\pi \, f_{HIGH} \, R_4} = 3.18 \, \mu F \tag{5}$$

Using a 2.2-nF capacitor, the upper cutoff frequency is 724 Hz.

R5 and C3 also cause the signal response to roll off. Therefore, it is beneficial to design this roll-off point to begin at the upper cutoff frequency. Assuming a value of 1 kΩ for R5, the value for C3 is calculated to be 0.22 µF.

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV277x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.

- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

- Sockets – Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.

- Short trace runs/compact part placements – Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

- Surface-mount passive components – Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

APPLICATION INFORMATION

general power dissipation considerations

For a given θ_{JA}, the maximum power dissipation is shown in Figure 63 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV277x IC (watts)

T_{MAX} = Absolute maximum junction temperature (150°C)

T_A = Free-ambient air temperature (°C)

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} = Thermal coefficient from junction to case

θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE

NOTE A.   Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 63. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

shutdown function

Three members of the TLV277x family (TLV2770/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 0.8 µA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, care needs to be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown. The shutdown terminal threshold is always referenced to $V_{DD}/2$. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not GND) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 48, 49, and 50. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables. The *bump* on the rising edge of the TLV2770 output waveform is due to the start-up circuit on the bias generator. For the dual and quad (TLV2773/5), this *bump* is attributed to the bias generator's start-up circuit as well as the cross talk between the other channel(s), which are in shutdown.

Figures 55 and 56 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35-V supplies and configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency for both 0.1 V_{PP} and 2.7 V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.7-V_{PP} input signal with a supply voltage of ±1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 4) and subcircuit in Figure 64 are generated using the TLV2772 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification

- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Intergrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).


```
.SUBCKT TLV2772–X 1 2 3 4 5
        C1      11   12   2.3094E–12          RD1     4    11   6.6315E3
        C2      6    7    8.0000E–12          RD2     4    12   6.6315E3
        CSS     10   99   2.1042E–12          R01     8    5    17.140
        DC      5    53   DY                  R02     7    99   17.140
        DE      54   5    DY                  RP      3    4    4.5455E3
        DLP     90   91   DX                  RSS     10   99   1.7182E6
        DLN     92   90   DX                  VB      9    0    DC 0
        DP      4    3    DX                  VC      3    53   DC .1
        EGND    99   0    POLY (2) (3,0) (4,0) 0 .5 .5    VE   54   4    DC .1
        FB      7    99   POLY (5) VB VC VE VLP          VLIM 7    8    DC 0
        + VLN 0 19.391E6 –1E3 1E3 19E6 –19E6            VLP  91   0    DC 47
        GA      6    0    11   12 150.80E–6    VLN     0    92   DC 47
        GCM     0    6    10   99 7.5576E–9    .MODEL DX D (IS=800.0E–18)
        ISS     3    10   DC 116.40E–6         .MODEL DY D (IS=800.0E–18 Rs = 1m Cjo=10p)
        HLIM    90   0    VLIM 1K              .MODEL JX1 PJF (IS=2.2500E–12 BETA=195.36E–6
        J1      11   2    10 JX1               + VTO=–1)
        J2      12   1    10 JX2               .MODEL JX2 PJF (IS=1.7500E–12 BETA=195.36E–6
        R2      6    9    100.00E3             + VTO=–1)
                                               .ENDS
```

Figure 64. Boyle Macromodel and Subcircuit

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General Information | 1

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Evaluation Modules | 4

Application Reports | 5

Mechanical Data | 6

3-1

Contents

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Product Previews

- 2.7-V and 5-V Performance
- Low Supply Current:
  LMV331 . . . 60 μA Typ
  LMV393 . . . 100 μA Typ
  LMV339 . . . 170 μA Typ
- Input Common-Mode Voltage Range
  Includes Ground
- Low Output Saturation Voltage
  . . . 200 mV Typ
- Package Options Include Plastic
  Small-Outline (D), Small-Outline Transistor
  (SOT-23 DBV, DCK), and Thin Shrink
  Small-Outline (PW) Packages
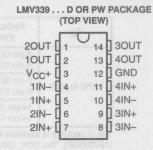
LMV339 . . . D OR PW PACKAGE
(TOP VIEW)

2OUT	1	14	3OUT
1OUT	2	13	4OUT
$V_{CC}+$	3	12	GND
1IN–	4	11	4IN+
1IN+	5	10	4IN–
2IN–	6	9	3IN+
2IN+	7	8	3IN–

LMV393 . . . D OR PW PACKAGE
(TOP VIEW)

1OUT	1	8	$V_{CC}+$
1IN–	2	7	2OUT
1IN+	3	6	2IN–
GND	4	5	2IN+

LMV331 . . . DBV OR DCK PACKAGE
(TOP VIEW)

IN+	1	5	$V_{CC}+$
V_{CC}–/GND	2		
IN–	3	4	OUT
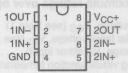
description

The LMV393 and LMV339 are low-voltage (2.7 V to 5.5 V) versions of the dual and quad comparators, LM393 and LM339, which operate from 5 V to 30 V. The LMV331 is the single-comparator version.
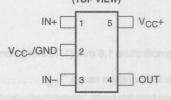
The LMV331, LMV339, and LMV393 are the most cost-effective solutions for applications where low-voltage operation, low power, space saving, and price are the primary specifications in circuit design for portable consumer products. These devices offer specifications that meet or exceed the familiar LM339 and LM393 devices at a fraction of the supply current.

The LMV331 is available in the ultra-small DCK package, which is approximately half the size of the five-pin SOT-23. The small package saves space on printer circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The LMV331, LMV339, and LMV393 devices are characterized for operation from –40°C to 85°C.

symbol (each comparator)

IN –

IN +

OUT

PRODUCT PREVIEW

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TEXAS INSTRUMENTS

AVAILABLE OPTIONS

TA	PACKAGE TYPE	PACKAGED DEVICES		
		SINGLE	**DUAL**	**QUADRUPLE**
−40°C to 85°C	5-pin DCK	LMV331DCKR	—	—
	5-pin DBV	LMV331DBVR	—	—
	8-pin SOIC	—	LMV393D	—
	8-pin TSSOP	—	LMV393PW	—
	14-pin SOIC	—	—	LMV339D
	14-pin TSSOP	—	—	LMV339PWR

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LMV393DR). The DCK, DBV, and PW packages are only available left-end taped and reeled.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 5.5 V
Differential input voltage, V_{ID} (see Note 2) .... ±5.5 V
Input voltage, V_I (either input) .... 0 to 5.5°C
Operating virtual junction temperature temperature range .... 0 to 150°C
Package thermal impedance, θ_{JA} (see Notes 3 and 4): D (8-pin) package .... 197°C/W
D (14-pin) package .... 127°C/W
DBV package .... 347°C/W
DCK package .... 389°C/W
PW (8-pin) package .... 243°C/W
PW (14-pin) package .... 170°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or PW package .... 260°C
DBV or DCK package .... TBD
Storage temperature range, T_{stg} .... −65 to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
2. Differential voltages are at IN+ with respect to IN−.
3. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) − T_A)/\theta_{JA}$. Selecting the maximum of 150 °C can impact reliability.
4. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)	2.7	5.5	V
T_A	Operating free-air temperature	−40	85	°C

PRODUCT PREVIEW

![TEXAS INSTRUMENTS logo]

TEXAS INSTRUMENTS

electrical characteristics at specified free-air temperature, V_{CC} = 2.7 V, V–/GND = 0 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1.7	7	mV
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage		25°C		5		μV/°C
I_{IB}	Input bias current		25°C		10	250	nA
			–40°C to 85°C			400	
I_{IO}	Input offset current		25°C		5	50	nA
			–40°C to 85°C			150	
I_O	Output curent	$V_O \leq 1.5$ V	25°C	5	23		mA
	Output leakage curent		25°C		0.003		μA
			–40°C to 85°C			1	
V_{ICR}	Common-mode input voltage range		25°C		–0.1 to 2		V
V_{SAT}	Saturation voltage	$I_O \leq 1$ mA	25°C		200		mV
I_{CC}	Supply current	LMV331	25°C		40	100	μA
		LMV393 (both comparators)	25°C		70	140	
		LMV339 (all four comparators)	25°C		140	200	

switching characteristics T_A = 25°C, V_{CC} = 2.7 V, R_L = 5.1 kΩ, V–/GND = 0 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay, high- to low-level output switching	Input overdrive = 10 mV		1000		ns
		Input overdrive = 100 mV		350		
t_{PLH}	Propagation delay, low- to high-level output switching	Input overdrive = 10 mV		500		ns
		Input overdrive = 100 mV		400		

electrical characteristics at specified free-air temperature, V_{CC} = 5 V, V–/GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		25°C		1.7	7	mV
			–40°C to 85°C			9	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage		25°C		5		µV/°C
I_{IB}	Input bias current		25°C		25	250	nA
			–40°C to 85°C			400	
I_{IO}	Input offset current		25°C		2	50	nA
			–40°C to 85°C			150	
I_O	Output curent	$V_O \leq 1.5$ V	25°C	10	84		mA
	Output leakage curent		25°C		0.003		µA
			–40°C to 85°C			1	
V_{ICR}	Common-mode input voltage range		25°C		–0.1 to 4.2		V
V_{SAT}	Saturation voltage	$I_O \leq 4$ mA	25°C		200	400	mV
			–40°C to 85°C			700	
I_{CC}	Supply current	LMV331	25°C		60	120	µA
			–40°C to 85°C			150	
		LMV393 (both comparators)	25°C		100	200	
			–40°C to 85°C			250	
		LMV339 (all four comparators)	25°C		170	300	
			–40°C to 85°C			350	

switching characteristics at specified free-air temperature , T_A = 25°C, V_{CC} = 5 V, R_L = 5.1 kΩ, V–/GND = 0V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay, high- to low-level output switching	Input overdrive = 10 mV		600		ns
		Input overdrive = 100 mV		200		
t_{PLH}	Propagation delay, low- to high-level output switching	Input overdrive = 10 mV		450		ns
		Input overdrive = 100 mV		300		

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

- **2.7-V and 5-V Performance**
- **No Crossover Distortion**
- **Low Supply Current:**
    LMV321 . . . 130 μA Typ
    LMV358 . . . 210 μA Typ
    LMV324 . . . 410 μA Typ
- **Rail-to-Rail Output Swing**
- **Package Options Include Plastic Small-Outline (D), Small-Outline Transistor (SOT-23 DBV, DCK), and Thin Shrink Small-Outline (PW) Packages**
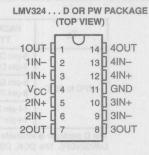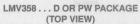
LMV324 . . . D OR PW PACKAGE
(TOP VIEW)

1OUT	1	14	4OUT
1IN–	2	13	4IN–
1IN+	3	12	4IN+
V_{CC}	4	11	GND
2IN+	5	10	3IN+
2IN–	6	9	3IN–
2OUT	7	8	3OUT

LMV358 . . . D OR PW PACKAGE
(TOP VIEW)

1OUT	1	8	$V_{CC}+$
1IN–	2	7	2OUT
1IN+	3	6	2IN–
GND	4	5	2IN+

LMV321 . . . DBV OR DCK PACKAGE
(TOP VIEW)

IN+	1	5	$V_{CC}+$
$V_{CC}–$/GND	2		
IN–	3	4	OUT

description

The LMV324 and LMV358 are low-voltage (2.7 V to 5.5 V) versions of the dual and quad commodity operational amplifiers, LM324 and LM358, that operate from 5 V to 30 V. The LMV321 is the single-amplifier version.
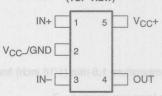
The LMV321, LMV324, and LMV358 are the most cost-effective solutions for applications where low-voltage operation, space saving, and low price are needed. They offer specifications that meet or exceed those of the familiar LM358 and LM324 devices. These devices have rail-to-rail output-swing capability, and the input common-mode voltage range includes ground. They all exhibit excellent speed-to-power ratios, achieving 1MHz of bandwidth at 1-V/μs slew rate with low supply current.

The LMV321 is available in the ultra-small DCK package, which is approximately half the size of the five-pin SOT-23. This package saves space on printed circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The LMV321, LMV324, and LMV358 devices are characterized for operation from –40°C to 85°C.

symbol (each amplifier)

IN – ——⟩
IN + ——⟩
—— OUT

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PRODUCT PREVIEW

TEXAS INSTRUMENTS

LMV321 SINGLE, LMV358 DUAL, LMV324 QUAD
OPERATIONAL AMPLIFIERS

AVAILABLE OPTIONS

T_A	PACKAGE TYPE	PACKAGED DEVICES		
		SINGLE	DUAL	QUADRUPLE
-40°C to 85°C	5-pin DCK	LMV321DCKR	—	—
	5-pin DBV	LMV321DBVR	—	—
	8-pin SOIC	—	LMV358D	—
	8-pin TSSOP	—	LMV358PW	—
	14-pin SOIC	—	—	LMV324D
	14-pin TSSOP	—	—	LMV324PWR

The D package is available taped and reeled. Add the suffix R to the device type (e.g., LMV324DR). The DCK, DBV, and PW packages are only available left-end taped and reeled.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) .... 5.5 V
Differential input voltage, V_{ID} (see Note 2) .... ±5.5 V
Input voltage, V_I (either input) .... 0 to 5.5 V
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25°C$,
 $V_{CC} \leq 5.5$ V (see Note 3) .... Unlimited
Operating virtual junction temperature temperature range) .... 150 °C
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D (8-pin) package .... 197 °C/W
 D (14-pin) package .... 127 °C/W
 DBV package .... 347 °C/W
 DCK package .... 389 °C/W
 PW (8-pin) package .... 243 °C/W
 PW (14-pin) package .... 170 °C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or PW package .... 260 °C
 DBV or DCK package .... TBD
Storage temperature range, T_{stg} .... -65 to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
2. Differential voltages are at IN+ with respect to IN–.
3. Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
4. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)	2.7	5.5	V
T_A	Operating free-air temperature	-40	85	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics at $T_A = 25°C$ and $V_{CC} = 2.7$ V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage				1.7	7	mV
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage				5		µV/°C
I_{IB}	Input bias current				11	250	nA
I_{IO}	Input offset current				5	50	nA
CMRR	Common-mode rejection ratio	$V_{CM} = 0$ to 1.7 V		50	63		dB
k_{SVR}	Supply-voltage rejection ratio	$V_{CC} = 2.7$ V to 5 V, $V_O = 1$ V		50	60		dB
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		0 to 1.7	−0.2 to 1.9		V
	Output swing	$R_L = 10$ kΩ to 1.35 V	High level	$V_{CC} - 100$	$V_{CC} - 10$		mV
			Low level		60	180	
I_{CC}	Supply current	LMV321			80	170	µA
		LMV358 (both amplifiers)			140	340	
		LMV324 (all four amplifiers)			260	680	
B_1	Unity-gain bandwidth	$C_L = 200$ pF			1		MHz
Φ_m	Phase margin				60		deg
G_m	Gain margin				10		dB
V_n	Equivalent input noise voltage	$f = 1$ kHz			46		nV/√Hz
I_n	Equivalent input noise current	$f = 1$ kHz			0.17		pA/√Hz

TEXAS INSTRUMENTS

PRODUCT PREVIEW

electrical characteristics at specified free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage			25°C		1.7	7	mV
				−40°C to 85°C			9	
$\alpha_{V_{IO}}$	Average temperature coefficient of input offset voltage			25°C		5		μV/°C
I_{IB}	Input bias current			25°C		15	250	V
				−40°C to 85°C			500	
I_{IO}	Input offset current			25°C		5	50	V
				−40°C to 85°C			150	
CMRR	Common-mode rejection ratio	V_{CM} = 0 to 4 V		25°C	50	65		V
k_{SVR}	Supply-voltage rejection ratio	V_{CC}= 2.7 V to 5 V, V_O = 1 V, V_{CM} = 1 V		25°C	50	60		V
V_{ICR}	Common-mode input voltage range	CMMR ≥ 50 dB		25°C	0 to 4	−0.2 to 4.2		V
	Output swing	R_L = 2 kΩ to 2.5 V	High level	25°C	V_{CC}–300	V_{CC}–40		mV
				−40°C to 85°C	V_{CC}–400			
			Low level	25°C		120	300	
				−40°C to 85°C			400	
		R_L = 10 kΩ to 2.5 V	High level	25°C	V_{CC}–100	V_{CC}–10		
				−40°C to 85°C	V_{CC}–200			
			Low level	25°C		65	180	
				−40°C to 85°C			280	
A_V	Large-signal voltage gain	R_L = 2 kΩ		25°C	15	100		V/mV
				−40°C to 85°C	10			
I_{OS}	Output short-circuit current	Sourcing, V_O = 0 V		25°C	5	60		V
		Sinking, V_O = 5 V			10	160		
I_{CC}	Supply current	LMV321		25°C		130	250	μA
		LMV358 (both amplifiers)		25°C		210	440	
		LMV324 (all four amplifiers)		−40°C to 85°C			1160	
B_1	Unity-gain bandwidth	C_L = 200 pF		25°C		1		MHz
Φ_m	Phase margin			25°C		60		deg
G_m	Gain margin			25°C		10		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		39		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.21		pA/√Hz
SR	Slew rate			25°C		1		V/μs

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Evaluation Modules

INTRODUCTION TO EVALUATION MODULES

The Universal Op Amp Evaluation Module is a printed circuit board (PCB) that greatly reduces design time, intended for quick evaluation of TI general purpose and performance amplifiers. See respective databooks for Audio Power or High Speed Amplifier EVMs.

To obtain a universal EVM board and amplifier samples for evaluation, select the appropriate EVM board from the Universal Op Amp Evaluation Module Selection Guide and contact your local TI sales office, distributor, or the TI Product Information Center (listed on the last page of this book). Evaluation modules will be introduced in the future. Please check the web (**www.ti.com**) for the latest updates and manuals.

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Universal Op Amp Evaluation Module Selection Guide

The Universal Op Amp Evaluation Module is a printed circuit board (PCB) that greatly reduces design time, intended for quick evaluation of TI general purpose and performance amplifiers. See respective databooks for Audio Power or High Speed Amplifier EVMs. The purpose of this guide is to show which universal EVM accomodates which amplifier package (also see **www.ti.com**).

	Shutdown	Package	Universal Op-Amp EVM SLOP120[1]	Universal Op-Amp EVM SLOP224[2]	Universal Op-Amp EVM SLOP247[3]	Universal Op-Amp EVM SLOP248[4]	Universal Op-Amp EVM SLOP249[5]
SINGLE	Without Shutdown	PDIP					X (8-pin)
		SOIC				X (8-pin)	
		SOT-23	X (5-pin)				
		TSSOP					
		MSOP			X (8-pin)		
	With Shutdown	PDIP					X (8-pin)
		SOIC		X (8-pin)		X (8-pin)	
		SOT-23		X (6-pin)			
		TSSOP					
		MSOP			X (8-pin)		
DUAL	Without Shutdown	PDIP					X (8-pin)
		SOIC	X (8-pin)			X (8-pin)	
		SOT-23					
		TSSOP					
		MSOP	X (8-pin)				
	With Shutdown	PDIP					X (14-pin)
		SOIC		X (14-pin)		X (14-pin)	
		SOT-23					
		TSSOP					
		MSOP		X (10-pin)	X (10-pin)		
QUAD	Without Shutdown	PDIP					X (14-pin)
		SOIC				X (14-pin)	
		SOT-23					
		TSSOP			X (14-pin)		
		MSOP					
	With Shutdown	PDIP				X (16-pin)	X (16-pin)
		SOIC					
		SOT-23					
		TSSOP			X (16-pin)		
		MSOP					

1. SLOP120 EVM Manual (SLVU006), orderable part number (UNIV–OPAMP–1B)
2. SLOP224 EVM Manual (SLVU009), orderable part number (UNIV–OPAMP–2B)
3. SLOP247 EVM Manual (SLOU055), orderable part number (UNIV–OPAMP–3B)
4. SLOP248 EVM Manual (SLOU061), orderable part number (UNIV–OPAMP–4B)
5. SLOP249 EVM Manual (SLOU062), orderable part number (UNIV–OPAMP–5B)

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Application Reports

Effect of Parasitic Capacitance in Op Amp Circuits

Application Report

James Karki

Literature Number: SLOA013
February 1999

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Effect of Parasitic Capacitance in Op Amp Circuits

James Karki

ABSTRACT

Parasitic capacitors are formed during normal op amp circuit construction. Op amp design guidelines usually specify connecting a small 20-pF to 100-pF capacitor between the output and negative input, and isolating capacitive loads with a small, 20-Ω to 100-Ω resistor. This application report analyzes the effects of capacitance at the input and output pins of an op amp, and suggests means for computing appropriate values for specific applications. The inverting and noninverting amplifier configurations are used for demonstration purposes. Other circuit topologies can be analyzed in a similar manner.

1 Introduction

Two conductors, insulated from one another, carrying a charge, and having a voltage potential between them, form a capacitor. Capacitors are characterized by their charge-to-voltage ratio; $C = \dfrac{q}{V}$, where C is the capacitance in Farads, q is the charge in Coulombs, and V is the voltage in volts. In general, capacitance is a function of conductor area, distance between the conductors, and physical properties of the insulator. In the special case of two parallel plates separated by an insulator $C = \dfrac{\epsilon\epsilon_0 \times A}{d}$ where ϵ is the dielectric constant of the insulator, ϵ_0 is the permittivity of free space, A is the area of the plates, and d is the distance between the plates. Thus, in general:

- Capacitance is directly proportional to the dielectric constant of the insulating material and area of the conductors.

- Capacitance is inversely proportional to the distance separating the conductors.

Rarely are two parallel plates used to make a capacitor, but in the normal construction of electrical circuits, an unimaginable number of capacitors are formed. On circuit boards, capacitance is formed by parallel trace runs, or traces over a ground or power plane. In cables there is capacitance between wires, and from the wires to the shield.

- Circuit traces on a PCB with a ground and power plane will be about 1–3 pF/in.

- Low capacitance cables are about 20–30 pF/ft conductor to shield.

Therefore, with a few inches of circuit board trace and the terminal capacitance of the op amp, it is conceivable that there can be 15–20 pF on each op amp terminal. Also, cables as short as a few feet can present a significant capacitance to the op amp.

This report assumes that a voltage feedback op amp is being used.

2 Basic One-Pole Op Amp Model

The voltage feedback op amp is often designed using dominant pole compensation. This gives the op amp a one-pole transfer function over the normal frequencies of operation that can be approximated by the model shown in Figure 1 (a). This model is used throughout this report in the spice simulations with the following values: $gm= 0.1$, $Rc= 1\,M\Omega$ and $Cc= 159\,nF$. With these values, the model has the following characteristics: dc gain = 100 dB, dominant pole frequency = 10 Hz, and unity gain bandwidth = 1 MHz.

In the schematic drawings, the representation shown in Figure 1 (b) is used, where $a = gm \times \dfrac{R_c}{1 + sRcCc}$.

(a) Spice Analysis Model (b) Schematic Representation
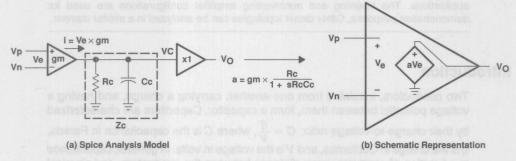
Figure 1. Basic Dominant Pole Op Amp Model

3 Basic Circuits and Analysis

Figure 2 (a) shows a noninverting amplifier and Figure 2 (b) shows an inverting amplifier. Both amplifier circuits are constructed by adding negative feedback to the basic op amp model.

(a) Noninverting Amplifier (b) Inverting Amplifier
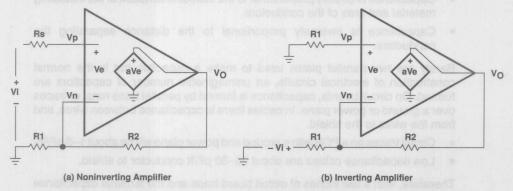
Figure 2. Amplifier Circuits Constructed with Negative Feedback

These circuits are represented in gain block diagram form as shown in Figure 3 (a) and (b). Gain block diagrams are a powerful tool in understanding gain and stability analysis.

(a) Noninverting Amplifier   (b) Inverting Amplifier
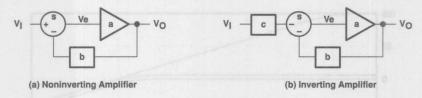
Figure 3. Gain-Block Diagrams

In the gain block diagrams:

$$a = gm \times \frac{R_c}{1 + sRcCc}, \quad b = \frac{R1}{R1 + R2}, \quad and \quad c = \frac{R2}{R1 + R2}.$$ Summing node s either inverts or passes unchanged each input—depending on the sign at the input—and adds the results together to produce the output.

3.1 Gain Analysis

In the gain block diagram of Figure 3 (a) (noninverting amplifier), Vo=aVe=a(Vi–bVo). Solving the transfer function:

$$\frac{V_O}{V_I} = \left(\frac{1}{b}\right)\left[\frac{1}{1 + \frac{1}{ab}}\right] = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)}\right] \tag{1}$$

This equation describes a single pole transfer function where $\frac{1}{b}$ is the dc gain and the pole is at the frequency where $\frac{1}{ab} = 1$

In the gain block diagram of Figure 3 (b) (inverting amplifier), $Vo = aVe = a(-cVi - bVo)$. Solving the transfer function:

$$\frac{V_O}{V_I} = -\left(\frac{c}{b}\right)\left[\frac{1}{1 + \frac{1}{ab}}\right] = \left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)}\right] \tag{2}$$

This equation describes a single pole transfer function where $-\frac{c}{b}$ is the dc gain and the pole is at the frequency where $\frac{1}{ab} = 1$.

Figure 4 shows the results of a spice simulation of the circuits with $R1$ and $R2 = 100$ kΩ, and $Rs = 50$ kΩ. As expected, the circuit gains are flat from dc to the point where $\frac{1}{ab} = 1$, and then roll-off at −20dB/dec. The open loop gain is plotted for reference.
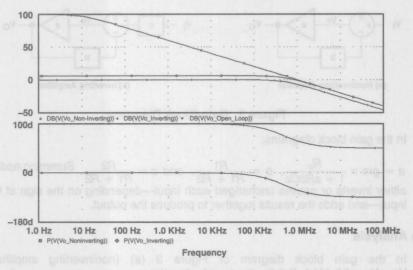
Figure 4. Spice Simulation of Noninverting and Inverting Amplifier

3.1.1 Stability Analysis

Using either gain block diagram, consider a signal traversing the loop from Ve, through the gain block a, to Vo, back through the gain block b, and the summing node s to Ve. If, while traversing this loop, the signal experiences a phase shift of 0°, or any integer multiple of 360°, and a gain equal to or greater than 1, it will reinforce itself causing the circuit to oscillate. Since there is a phase shift of 180° in the summing node s, this equates to:

$|ab| \geq 1 \& \angle ab = -180° \rightarrow Oscillation$.

In reality, anything close to this usually causes unacceptable overshoot and ringing.

The product of the open loop gain of the op amp, a, and the feedback factor, b, is of special significance and is often termed the loop gain or the loop transmission. To determine the stability of an op amp circuit, consider the magnitude, $|ab|$, and phase, $\angle ab$.

Figure 5 shows dB $|a|$ and dB $\frac{1}{b}$ plotted along with $\angle ab$ for the one-pole op amp model in either amplifier circuit with purely resistive feedback (R1=R2=100K). It is obvious that, since the maximum phase shift in $\angle ab$ is −90°, the circuits are stable.
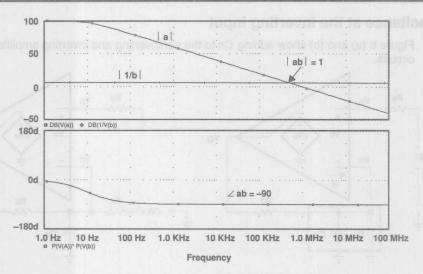
Figure 5. Loop Gain Magnitude and Phase Plot

At the point where dB |a| and dB $\left|\dfrac{1}{b}\right|$ intersect, dB |a| − dB $\left|\dfrac{1}{b}\right|$ = 0. This is the same as *log* |a| + *log* |b| = 0, and taking the anti-log; |*ab*| = *1*.

The slope of dB |a| or dB $\left|\dfrac{1}{b}\right|$ indicates their phase: −40 dB/dec = −180°, −20 dB/dec = −90°, 0 dB/dec = 0°, 20 dB/dec = 90°, 40 dB/dec = 180°, etc. Since $\left|\dfrac{1}{b}\right|$ is the inverse of |b|, the sign of its phase is opposite, i.e., if $\angle b$=−90° then $\angle \dfrac{1}{b}$ = 90°. Therefore a rate of closure = 40 dB/dec between dB |a| and dB $\left|\dfrac{1}{b}\right|$ indicates $\angle ab$=−180° and the circuit is normally unstable. Plotting dB |a| and dB $\left|\dfrac{1}{b}\right|$ on a log scale gives a visual indication of the stability of the circuit.

4 Capacitance at the Inverting Input

Figure 6 (a) and (b) show adding Cn to the noninverting and inverting amplifier circuits.

(a) Noninverting Amplifier   (b) Inverting Amplifier
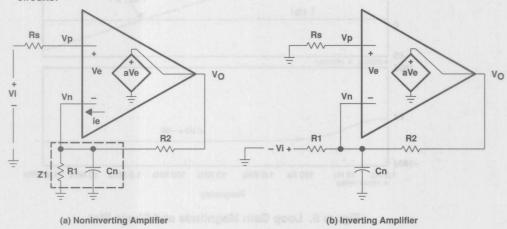
Figure 6. Adding Cn to Amplifier Circuits

4.1 Gain Analysis with Cn

Making use of the block diagrams and their related circuit solutions, determine how Cn has modified the gain block values and substitute as required.

For the noninverting amplifier shown in Figure 6 (a):

$$Vn = Vo\frac{Z1}{Z1 + R2}$$

where $Z1 = \dfrac{R1}{1 + sR1\,Cn}$.

Solving for the modified feedback factor:

$$b = \frac{Z1}{Z1 + R2} = \left(\frac{R1}{1 + sR1\,Cn}\right)\left[\frac{1}{\left(\frac{R1}{1 + sR1\,Cn}\right) + R2}\right] = \frac{1}{\frac{R1 + R2}{R1} + sR2\,Cn} \tag{3}$$

For the inverting amplifier shown in Figure 6 (b) writing the node equation at Vn results in:

$$\frac{Vn{-}Vi}{R1} + Vn{\times}sCn + \frac{Vn{-}Vo}{R2} = 0.$$

Therefore,

$$Vn = Vi\left(\frac{R2}{R1 + R2 + sCnR1R2}\right) + \left(\frac{Vo(R1)}{R1 + R2 + sCnR1R2}\right)$$

$$= Vi\left[\frac{1}{\dfrac{R1+R2}{R2} + sCnR1}\right] + Vo\left[\frac{1}{\dfrac{R1+R2}{R1} + sCnR2}\right]$$

As above:

$$b = \frac{1}{\dfrac{R1+R2}{R1} + sR2Cn}, \quad and \quad c = \frac{1}{\dfrac{R1+R2}{R2} + sR2Cn}$$

Using these values in the solutions to the gain block diagrams of Figure 3, the noninverting amplifier's gain, with Cn added to the circuit, is:

$$\frac{Vo}{Vi} = \left(\frac{1}{b}\right)\left[\frac{1}{1 + \dfrac{1}{ab}}\right] = \left(\frac{R1+R2}{R1} + sR2Cn\right)\left[\frac{1}{1 + \left(\dfrac{1+sRcCc}{gmRc}\right)\left(\dfrac{R1+R2}{R1} + sR2Cn\right)}\right] \quad (4)$$

and the inverting amplifier's gain, with Cn added to the circuit, is:

$$\frac{Vo}{Vi} = -\left(\frac{c}{b}\right)\left[\frac{1}{1 + \dfrac{1}{ab}}\right] = -\left[\frac{\dfrac{R1+R2}{R1} + sR2Cn}{\dfrac{R1}{\dfrac{R1+R2}{R2}+sR1Cn}}\right]\left[\frac{1}{1 + \left(\dfrac{1+sRcCc}{gmRc}\right)\left(\dfrac{R1+R2}{R1} + sR2Cn\right)}\right] \quad (5)$$

$$= -\left(\frac{R2}{R1}\right)\left[\frac{\dfrac{R1+R2}{R2}+sR1Cn}{\dfrac{R1+R2}{R2}+sR1Cn}\right]\left[\frac{1}{1 + \left(\dfrac{1}{a}\right)\left(\dfrac{R1+R2}{R1} + sR2Cn\right)}\right]$$

$$= -\left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \left(\dfrac{1+sRcCc}{gmRc}\right)\left(\dfrac{R1+R2}{R1} + sR2Cn\right)}\right]$$

Figure 7 shows the results of a spice simulation of both amplifiers with $Cn = 15.9$ nF, resistors $R1$ and $R2 = 100$ kΩ, and $Rs = 50$ kΩ. Refer to it while taking a closer look at Equations 4 and 5.

In Equation 4, the first term

$$\left(\frac{R1+R2}{R1} + sR2Cn\right)$$

contains a zero at

$$f_z = \frac{R1+R2}{2\pi R1R2Cn}.$$

In the spice simulation we see effects of this zero as the gain begins to increase at around 200 Hz. In the second term of Equation 4, substitute

$Rm = \dfrac{1}{gm}$, to get

$$\left[\dfrac{1}{1 + \left(\dfrac{Rm}{Rc} + sRmCc\right)\left(\dfrac{R1 + R2}{R1} + sR2Cn\right)} \right]$$

$$= \dfrac{1}{s^2(RmCcR2Cn) + s\left(R2Cn\dfrac{Rm}{Rc} + RmCc\dfrac{R1 + R2}{R1}\right) + 1 + \left(\dfrac{Rm}{Rc}\right)\left(\dfrac{R1 + R2}{R1}\right)}$$

Solving the characteristic equation for s^2 in the denominator we find that the transfer function has a complex conjugate pole at $s_{1,2} = -660 \pm j62890$. Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain at:

$$P_{1,2} = \dfrac{1}{2\pi\sqrt{RmCcR2Cn}} = 10\ kHz,$$

with the model values as simulated. At this frequency the denominator tends to zero and the gain theoretically increases toward infinity. What we see on the simulation results is peaking in the gain plot and a rapid 180° phase shift in the phase plot at 10 kHz. The circuit is unstable.

In Equation 5, notice that the frequency effects of the capacitor cancel out of the first term of the transfer function. The simulation results show the gain is flat until the second term, which is identical to Equation 4, causes peaking in the gain plot, and a rapid 180° phase shift in the phase plot at 10 kHz. This circuit is also unstable.
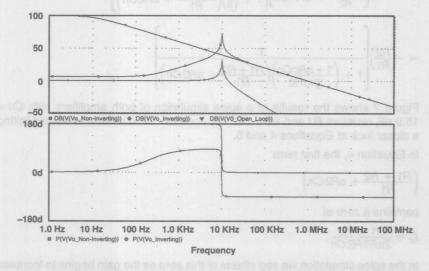
Figure 7. Spice Simulation of *Cn* in Noninverting and Inverting Amplifiers

4.1.1 Stability Analysis with Cn

To analyze stability with Cn added to the amplifier circuit, use the modified feedback factor,

$$b = \cfrac{1}{\cfrac{R1 + R2}{R1} + sR2Cn}$$

At low frequencies where

$$\frac{R1 + R2}{R1} >> 2\pi fR2Cn, \frac{1}{b} \cong \frac{R1 + R2}{R1}$$

and the plot is flat ($\angle b = 0°$). As frequency increases, eventually $\frac{R1 + R2}{R1} = 2\pi fR2Cn$. At this frequency $\left|\frac{1}{b}\right| = \left(\frac{R1 + R2}{R1}\right)\left(\sqrt{2}\right)$ ($\angle b = -45°$).

Above this frequency $\left|\frac{1}{b}\right|$ increases at 20dB/dec ($\angle b = -90°$). Depending on the value of Cn, there are two possible scenarios:

1. The break frequency is below the frequency where $\left|\frac{1}{b}\right|$ and $|a|$ intersect. This causes the rate of closure between $\left|\frac{1}{b}\right|$ and $|a|$ to be 40dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference $\frac{1}{b1}$ in Figure 8 and the results of the spice simulation shown in Figure 7.

2. The break frequency is above the frequency where $\left|\frac{1}{b}\right|$ and $|a|$ intersect. There is no effect in the pass band of the amplifier. Reference $\frac{1}{b2}$ in Figure 8.
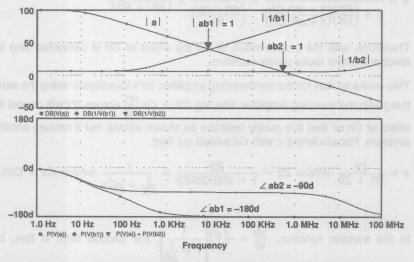
Figure 8. Loop Gain Magnitude and Phase Asymptote Plots with Cn

4.1.2 Compensating for the Effects of Cn

1. Reduce the value of Cn by removing ground or power plane around the circuit trace to the inverting input.

2. Reduce the value of $R2$.

3. For noninverting amplifier, place a capacitor $C2 = Cn\dfrac{R1}{R2}$ in parallel with $R2$.

4. For inverting amplifier, place a capacitor $C2 = Cn\dfrac{R1}{R2}$ in parallel with $R2$, and place a capacitor $C1 = Cn$ in parallel with $R1$.

Methods 1 and 2 attempt to move the effect of Cn to a higher frequency where it does not interfere with normal operation.

Method 3 is used for the noninverting amplifier. It cancels the effect of Cn.

To solve the modified transfer function with $C2$ in parallel with $R2$, substitute $Z2$ for $R2$, where $Z2 = \dfrac{R2}{1 + sR2C2}$, in the derivation of b so that:

$$b = \frac{Vn}{Vo} = \frac{Z1}{Z1 + Z2} = \frac{\left(\dfrac{R1}{1 + sR1\,Cn}\right)}{\left(\left(\dfrac{R1}{1 + sR1\,Cn}\right) + \left(\dfrac{R2}{1 + sR2C2}\right)\right)} = \frac{1}{1 + \left(\dfrac{R2}{R1}\right)\left(\dfrac{1 + sR1\,Cn}{1 + sR2C2}\right)} \tag{6}$$

By setting $C2 = Cn\dfrac{R1}{R2}$, Equation 6 becomes:

$$b = \frac{1}{1 + \left(\dfrac{R2}{R1}\right)\left(\dfrac{1 + sR1\,Cn}{1 + sR1\,Cn}\right)} = \frac{1}{\left(\dfrac{R1 + R2}{R1}\right)} = \left(\frac{R1}{R1 + R2}\right).$$

Therefore, with the proper value of $C2$ the effect of Cn is cancelled and the feedback factor looks purely resistive.

This works so well for the noninverting amplifier, let's investigate doing the same thing with the inverting amplifier. Placing $C2 = Cn\dfrac{R1}{R2}$ across $R2$ will cancel the effect of Cn so that b is purely resistive as shown above, but it causes another problem. Recalculating c with $C2$ added we find:

$$c = \frac{Z2}{R1 + Z2} \quad \text{where } Z2 = \frac{R2}{1 + sR2C2\|Cn} = \frac{1}{\dfrac{1}{R2} + sCx} \quad \text{where } Cx = C2\|Cn.$$

In the transfer function, $\dfrac{Vo}{Vi} = -\left(\dfrac{c}{b}\right)\left[\dfrac{1}{1 + \dfrac{1}{ab}}\right]$, the second term is fine, but expanding out the first term we find:

$$\left(\frac{c}{b}\right) = \left(\frac{R2}{1 + sR2Cx}\right)\left[\frac{1}{R1 + \frac{R2}{1 + sR2Cx}}\right]\left(\frac{R1 + R2}{R1}\right) = \left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \frac{sR1R2Cx}{R1 + R2}}\right]$$

Obviously we now have a pole in the transfer function at $f_p = 2\pi Cx\left(\frac{R1 + R2}{R1R2}\right)$ that limits the circuit's bandwidth. To cancel this pole, a zero needs to be added to the transfer function. Placing a capacitor, *C1*, across *R1* will create a zero in the transfer function.

Again c and b need to be recalculated. We already have the solution in the form of Equation 6, and by proper substitution:

$$b = \frac{Vn}{Vo} = \left[\frac{\left(\frac{R1}{1 + sR1\,Cn\|C1}\right)}{\left(\left(\frac{R1}{1 + sR1\,Cn\|C1}\right) + \left(\frac{R2}{1 + sR2C2}\right)\right)}\right] = \frac{1}{1 + \left(\frac{R2}{R1}\right)\left(\frac{1 + sR1\,Cn\|C1}{1 + sR2C2}\right)} \tag{7}$$

$$c = \frac{Vn}{Vi} = \left[\frac{\left(\frac{R2}{1 + sR2\,Cn\|C2}\right)}{\left(\left(\frac{R2}{1 + sR2\,Cn\|C2}\right) + \left(\frac{R1}{1 + sR1\,C1}\right)\right)}\right] = \frac{1}{1 + \left(\frac{R1}{R2}\right)\left(\frac{1 + sR2\,Cn\|C2}{1 + sR1\,C1}\right)}$$

$$\left(\frac{c}{b}\right) = \frac{1 + \left(\frac{R2}{R1}\right)\left(\frac{1 + sR1\,Cn\|C1}{1 + sR2C2}\right)}{1 + \left(\frac{R1}{R2}\right)\left(\frac{1 + sR2\,Cn\|C2}{1 + sR1\,C1}\right)}$$

Setting $C2 = (Cn\|C1)\frac{R1}{R2}$ in the numerator, simultaneously with setting $C1 = (Cn\|C2)\frac{R2}{R1}$ in the denominator, results in cancellation. The problem is that this cannot be simultaneously achieved.

To arrive at a suitable compromise, assume that placing $C2 = Cn\frac{R1}{R2}$ across *R2* cancels the effect of *Cn* in the feedback path as described above. Then, isolate the signal path between *Vi* and *Vn* by assuming *R2* is open. With this scenario, *Cn* is acting with *R1* to create a pole in the input signal path and placing an equal value capacitor in parallel with *R1* will create a zero to cancel its effect.

Figure 9 shows the results of a spice simulation where methods 3 and 4 are used to compensate for *Cn* = 15.9 nF. *C2* = 15.9 F in the noninverting amplifier and *C1* = *C2* = 15.9 F in the inverting amplifier. In both amplifier circuits, resistors *R1* and *R2* = 100 kΩ, and *Rs* = 50 kΩ. The plots show excellent results.
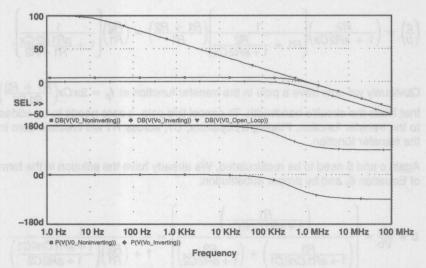
Figure 9. Simulation Results with C1 and C2 Added to Compensate for *Cn*

The action of any op amp operated with negative feedback is such that it tries to maintain 0 V across the input terminals. In the inverting amplifier, the op amp works to keep 0V (and thus 0 charge) across *Cn*. Because capacitance is the ratio of charge to potential, the effective capacitance of *Cn* is greatly reduced. In the noninverting amplifier *Cn* is charged and discharged in response to *Vi*. Thus the impact of *Cn* depends on topology. Lab results verify that, in inverting amplifier topologies, the effective value of *Cn* will be reduced by the action of the op amp, and tends to be less problematic than in noninverting topologies. Figure 10 shows that the effects of adding *Cn* to a noninverting amplifier are much worse than adding 10 times the same amount to an inverting amplifier with similar circuit components.
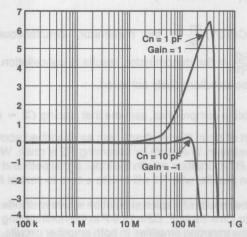
Figure 10. Effect of *Cn* in Inverting and Noninverting Amplifier

5 Capacitance at the Noninverting Input

In Figure 11 *Cp* is added to the amplifier circuits.

(a) Noninverting Amplifier   (b) Inverting Amplifier
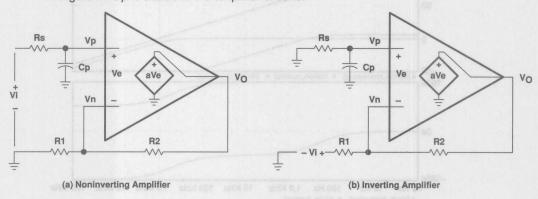
Figure 11. Adding *Cp* to Amplifier Circuits

5.1 Gain Analysis with *Cp*

In the case of the noninverting amplifier, the voltage seen at the noninverting input is modified so that $Vp = Vi\left(\dfrac{1}{1 + sRsCp}\right)$. Thus there is a pole in the input signal path before the signal reaches the input of the op amp. *Rs* and *Cp* form a low pass filter between *Vi* and *Vp*. If the break frequency is above the frequency at which $\left|\dfrac{1}{b}\right|$ intersects |a|, there is no effect on the operation of the circuit in the normal frequencies of operation.

The gain of the inverting amplifier is not affected by adding *Cp* to the circuit.

Figure 14 shows the results of a spice simulation where *Cp* = 15.9 nF. In both amplifier circuits, resistors *R1* and *R2* = 100 kΩ, and *Rs* = 50 kΩ. The plot shows a pole in the transfer function of the noninverting amplifier, whereas the inverting amplifier is unaffected.
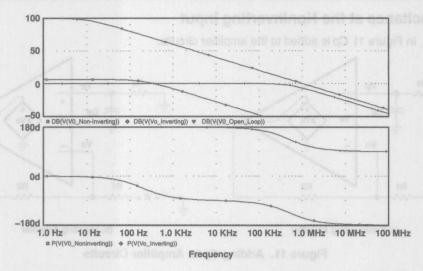
Figure 12. Spice Simulation with *Cp* in Noninverting and Inverting Amplifier Circuits

5.2 Stability Analysis with *Cp*

There is no change in the loop gain and thus no effect on stability for either amplifier circuit.

5.3 Compensating for the Effects of *Cp*

To compensate for the effect of capacitance at the noninverting input:

1. Reduce the value of *Cp* by removing ground or power plane around the circuit trace to the noninverting input.

2. Reduce the value of *Rs*.

3. Place a capacitor, *Cs,* in parallel with *Rs* so that *Cs>>Cp*.

Methods 1 and 2 attempt to move the effect of *Cp* to a higher frequency where it does not affect transmission of signals in the pass band of the amplifier.

Method 3 tries to cancel the effect of *Cp*. The modified transfer function with *Cs* in parallel with *Rs* is:

$$\frac{Vp}{Vi} = \left(\frac{1 + sRsCs}{1 + sRs(Cp + Cs)} \right)$$

(8)

If *Cs>>Cp*, then $\left(\dfrac{1 + sRsCs}{1 + sRs(Cp + Cs)} \right) \cong 1$ *and Vp ≅ Vi.*

Figure 13 shows the results of a spice simulation of the previous noninverting amplifier circuit where a 159-nF and a 1.59-µF capacitor is placed in parallel with *Rs* to compensate for *Cp* = 15.9 nf. The plot shows that a 10:1 ratio is good—loss of 1 db in gain at higher frequencies, but with a 100:1 ratio the effects of *Cp* are undetectable.
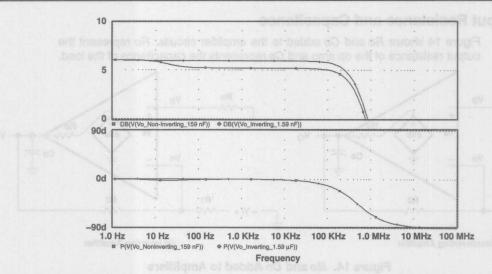
Figure 13. Spice Simulation with *Cs* Added to Compensate for *Cp* in Noninverting Amplifier

6 Output Resistance and Capacitance

Figure 14 shows *Ro* and *Co* added to the amplifier circuits. *Ro* represent the output resistance of the op amp and *Co* represents the capacitance of the load.

(a) Noninverting Amplifier (b) Inverting Amplifier
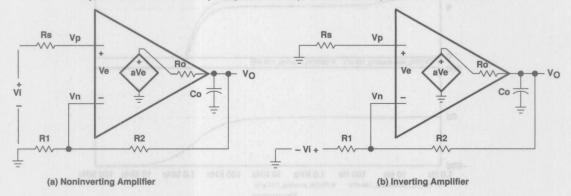
Figure 14. *Ro* and *Co* Added to Amplifiers

6.1 Gain Analysis with *Ro* and *Co*

Assuming that the impedance of *R2* is much higher than the impedance of *Ro* and *Co*, the gain block diagrams for the amplifiers are modified to those shown in Figure 15 where:

$$d = \frac{Vo}{aVe} = \frac{1}{1 + sRoCo}.$$

(a) Noninverting Amplifier (b) Inverting Amplifier
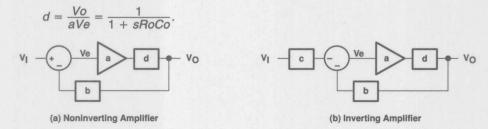
Figure 15. Gain Block Diagrams with *Ro* and *Co*

Using Figure 15 (a), we calculate the transfer function of the noninverting amplifier:

$$\frac{Vo}{Vi} = \frac{1}{b}\left[\frac{1}{1 + \frac{1}{abd}}\right] = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)(1 + sRoCo)}\right] \tag{9}$$

Using Figure 15 (b), we calculate the transfer function of the inverting amplifier:

$$\frac{Vo}{Vi} = -\left(\frac{c}{b}\right)\left[\frac{1}{1 + \frac{1}{abd}}\right] = -\left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)(1 + sRoCo)}\right] \tag{10}$$

Figure 16 shows the results of a spice simulation with Ro = 100 Ω and Co = 159 μF. Resistors $R1$ and $R2$ = 100 kΩ, and Rs = 50 kΩ. Refer to the simulation results while taking a closer look at the second term of Equations 9 and 10. Expanding the denominator of second term with $Rm = \frac{1}{gm}$ and collecting s terms:

$$s^2(RmCcRoCo)\left(\frac{R1 + R2}{R1}\right) + s\left(RoCo\left(\frac{Rm}{Rc}\right) + RmCc\right)\left(\frac{R1 + R2}{R1}\right) + 1 + \left(\frac{Rm}{Rc}\right)\left(\frac{R1 + R2}{R1}\right)$$

Solving the characteristic equation for s^2, the transfer function has a complex conjugate pole at $s_{1,2} = -63 + j14{,}063$. Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain at:

$$f_{p1,2} \cong \frac{1}{2\pi\sqrt{RmCcRoCo\left(\frac{R1 + R2}{R1}\right)}} = 2.2\ kHz,$$

with the model values as simulated. At this frequency the second term's denominator tends to zero and the gain theoretically increases to infinity. What we see on the simulation results at 2.2 kHz is significant peaking in the gain, and a rapid 180° phase shift. The circuit is unstable.
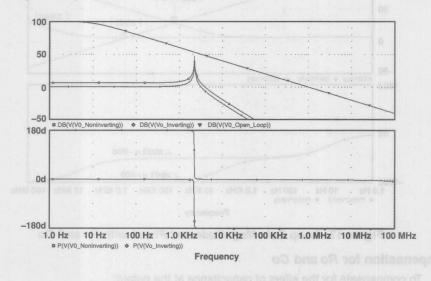
Figure 16. Spice Simulation with *Ro* and *Co*

6.2 Stability Analysis with *Ro* and *Co*

By the gain block diagrams shown in Figure 15 (a) and (b), the loop gain is now = *abd* for both circuits. Since gain blocks *a* and *b* are not changed, to determine the stability of the circuit, the effect of gain block *d* is analyzed.

As noted above, $d = \dfrac{Vo}{aVe} = \dfrac{1}{1 + sRoCo}$. At low frequencies where $1 >> 2\pi fRoCo, \dfrac{1}{d} \cong 1$ and the plot is flat ($\angle d = 0°$). As frequency increases, eventually $2\pi fRoCo = 1$. At this frequency $\left|\dfrac{1}{d}\right| = \left(\sqrt{2}\right)$, and $\angle d = -45°$. Above this frequency $\left|\dfrac{1}{d}\right|$ increases at 20dB/dec , and $\angle d = -90°$. Depending on the value of *Ro* and *Co*, there are two possible scenarios:

1. The break frequency is below the frequency where $\left|\dfrac{1}{bd}\right|$ and |a| intersect. This causes the rate of closure to be 40dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference $\left|\dfrac{1}{bd1}\right|$ in Figure 17 and the results of the spice simulation shown in Figure 16.

2. The break frequency is above the frequency where $\left|\dfrac{1}{bd}\right|$ and |a| intersect. There is no effect in the pass band of the amplifier. Reference $\left|\dfrac{1}{bd2}\right|$ in Figure 17.
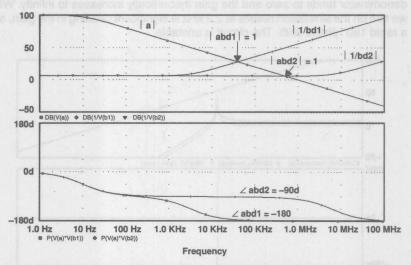
Figure 17. Loop Gain Magnitude and Phase with *Ro* and *Co*

6.3 Compensation for *Ro* and *Co*

To compensate for the effect of capacitance at the output:

1. Reduce the value of *Co* by removing ground or power plane around the circuit trace to the output.
2. Reduce the value of *Co* by minimizing the length of output cables.
3. Isolate the output pin from *Co* with a series resistor.
4. Isolate the output pin from *Co* with a series resistor, and provide phase lead compensation with a capacitor across *R2*.

Methods 1 and 2 seek to minimize the value of *Co* and thus its effects, but there is a limit to what can be done. In some cases, you will still be left with a capacitance that is too large for the amplifier to drive. Then method 3 or 4 can be used depending on your requirements.

Method 3 can be used if the resistive load is insignificant, or it is known and constant. Figure 18 shows the circuit modified with *Ri* added to isolate *Co*. By observation, adding Ri increases the phase shift seen at *Vo*, but now the feedback is taken from node *Vfb*.

(a) Noninverting Amplifier   (b) Inverting Amplifier
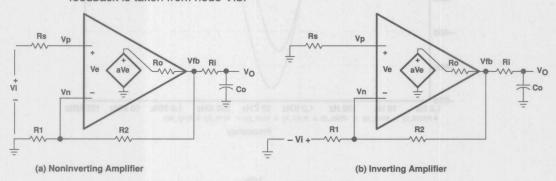
Figure 18. Isolation Resistor Added to Isolate the Feedback Loop from Effects of *Ro*

This modifies the gain block *d*. Making the assumption that the impedance of *Ro*, *Ri*, and *Co* is small compared to *R2* then:

$$d = \frac{Vfb}{aVe} = \left(\frac{Ri + \frac{1}{sCo}}{Ro + Ri + \frac{1}{sCo}} \right) = \frac{1}{\frac{Ro}{Ri} + 1 + \frac{1}{sRiCo}} + \frac{1}{1 + sCo(Ri + Ro)}.$$

Letting $z = \dfrac{1}{\frac{Ro}{Ri} + 1 + \frac{1}{sRiCo}}$ and $p = \dfrac{1}{1 + sCo(Ri + Ro)} : d = z + p.$ z is a

zero and p is a pole. Both have the same corner frequency; $f_{z,p} = \dfrac{1}{2\pi Co(Ri + Ro)}.$ When $f << f_{z,p}$, or when $f >> f_{z,p}$ the phase is zero. The ratio of *Ri:Ro* determines the maximum phase shift near $f_{z,p}$.

Figure 19 shows a plot of the phase shift of $\dfrac{Vfb}{aVe}$ versus frequency with various ratios of *Ri:Ro* and Figure 20 plots the maximum phase shift vs. the ratio of *Ri:Ro*. Depending on how much the phase margin can be eroded, a ratio can be chosen to suit. Note that the amount of phase shift depends only on the resistor ratio, not the resistor or capacitor values (these set the frequency $f_{z,p}$).
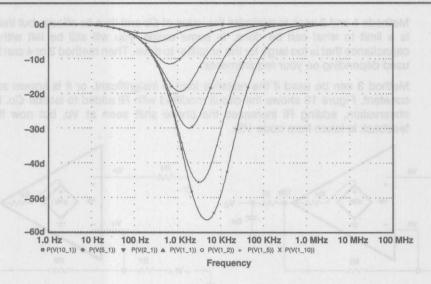
Figure 19. Phase Shift in $\frac{Vfb}{aVe}$ vs the Ratio *Ri:Ro*
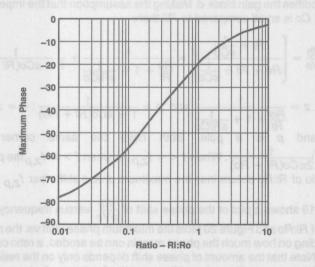
Figure 20. Maximum Phase Shift in $\frac{Vfb}{aVe}$ vs the Ratio *Ri:Ro*

Figure 21 shows simulation results with the same circuits as used for Figure 16 ($Ro = 100\,\Omega$ and $Co = 159\,\mu F$), but with $Ri = 100\,\Omega$ added to the circuit. The circuits are stable.

□ DB(V(Vo_Non_Inverting)) ◆ DB(V(Vo_Inverting)) ▼ DB(V(Vo_Open_Loop))

□ P(V(Vo_Non_Inverting)) ◆ P(V(Vo_Inverting))

Frequency
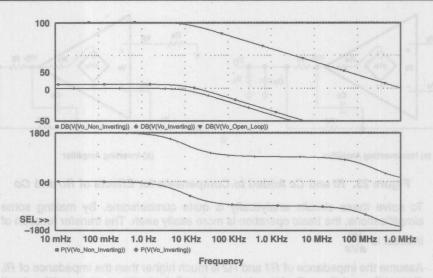
Figure 21. Spice Simulation Results with *Ri* Added to Compensate for *Ro* and *Co*

A common use of an isolation resistor is shown in Figure 22 where a video buffer circuit is drawn. To avoid line reflections, the signal is delivered to the transmission line through a 75-Ω resistor, and the transmission line is terminated at the far end with a 75-Ω resistor. To compensate for the voltage divider, the gain of the op amp is 2.
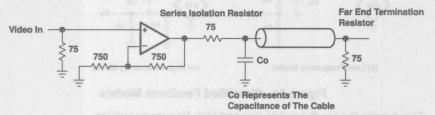
Figure 22. Video Buffer Application

If the load is unknown or dynamic in nature, method 3 is not satisfactory. Then method 4, the configuration shown in Figure 23, is used with better results. At low frequencies, the impedance of *Cc* is high in comparison with *R2*, and the feedback path is primarily from *Vo* restoring the dc and low frequency response. At higher frequencies, the impedance of *Cc* is low compared with *R2,* and the feedback path is primarily from *Vfb*, where the phase shift, due to *Co*, is buffered by *Ri*.

(a) Noninverting Amplifier

(b) Inverting Amplifier
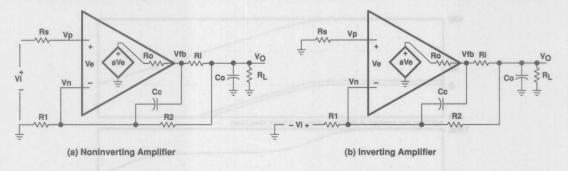
Figure 23. *Ri* and *Cc* Added to Compensate for Effects of *Ro* and *Co*

To solve these circuits analytically is quite cumbersome. By making some simplifications, the basic operation is more easily seen. The transfer function of interest is $\dfrac{Vn}{aVe}$.

Assume the impedance of *R1* and *R2* is much higher than the impedance of *Ri*, *Ro* and *Co*, and *Cc* << *Co*. At low frequencies, *Cc* looks like an open and the circuit can be represented as shown in Figure 24 (a). At higher frequencies *Cc* becomes active, *Co* is essentially a short, and the circuit can be represented as shown in Figure 24 (b).

(a) Low Frequency Model

(a) High Frequency Model

Figure 24. Simplified Feedback Models

This breaks the feedback into low and high frequency circuits:

At low frequency: $\dfrac{Vn}{aVe}\left(f_{low}\right) = \left(\dfrac{R1}{R1 + R2}\right)\left(\dfrac{1}{1 + sCo(Ro + Ri)}\right)$.

At high frequency: $\dfrac{Vn}{aVe}\left(f_{high}\right) = \left(\dfrac{Ri}{Ri + Ro}\right)\left[\dfrac{1}{1 + \dfrac{1}{sCc(R1\|R2)}}\right]$.

The overall feedback factor is a combination of the two so that:

$$\frac{Vn}{aVe} = \left(\frac{R1}{R1 + R2}\right)\left(\frac{1}{1 + sCo(Ro + Ri)}\right) + \left(\frac{Ri}{Ri + Ro}\right)\left[\frac{1}{1 + \dfrac{1}{sCc(Ro+Ri)}}\right]$$

This formula contains a pole and a zero. Choosing the value of the components so that the pole and zero are at the same frequency by setting $Cc = Co\dfrac{Ro + Ri}{R1\|R2}$ results in the feedback path switching from *Vo* to *Vfb* as the phase shift due to *Co(Ri+Ro)* transitions to −90°.

Figure 24 shows the simulation results of adding *Cc* = 636 nf with isolation resistor, *Ri* = 100 Ω, to the feedback path (as indicated in Figure 23). The circuit is no longer unstable and the low frequency load independence of the output is restored. Simulation of the circuit shows similar results as those depicted in Figure 21, and is not shown.
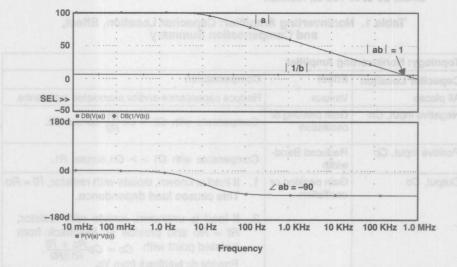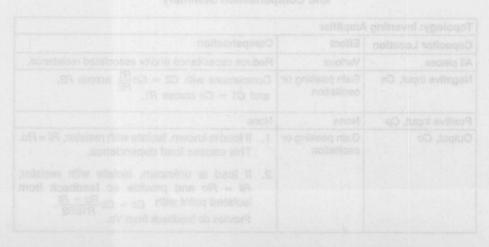
Figure 25. Simulation of Feedback Using *Ri* and *Cc* to Compensate for *Ro* and *Co*

7 Summary

The techniques described herein show means for analyzing and compensating for known component values. In circuit application, the value of parasitic components is not always known. Thus the ubiquitous rule of thumb comes into play:

1. Always connect a small, 20-pF to 100-pF, capacitor between the output and the negative input.

2. If the op amp has to drive a significant capacitance, isolate the output with a small, 20-Ω to 100-Ω, resistor.

Table 1. Noninverting Amplifier: Capacitor Location, Effect, and Compensation Summary

Topology: Noninverting Amplifier		
Capacitor Location	**Effect**	**Compensation**
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, Cn	Gain peaking or oscillation	Compensate with $C2 = Cn\dfrac{R1}{R2}$ across $R2$.
Positive input, Cp	Reduced Bandwidth	Compensate with $C1 >> Cn$ across $R1$.
Output, Co	Gain peaking or oscillation	1. If load is known, isolate with resistor, $Ri = Ro$. This causes load dependence. 2. If load is unknown, isolate with resistor, $Ri = Ro$ and provide ac feedback from isolated point with $Cc = Co\dfrac{Ro + Ri}{R1\|R2}$. Provide dc feedback from Vo.

Table 2. Inverting Amplifier: Capacitor Location, Effect, and Compensation Summary

Topology: Inverting Amplifier		
Capacitor Location	**Effect**	**Compensation**
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, Cn	Gain peaking or oscillation	Compensate with $C2 = Cn\dfrac{R1}{R2}$ across $R2$, and $C1 = Cn$ across $R1$.
Positive input, Cp	None	None
Output, Co	Gain peaking or oscillation	1. If load is known, isolate with resistor, $Ri = Ro$. This causes load dependence. 2. If load is unknown, isolate with resistor, $Ri = Ro$ and provide ac feedback from isolated point with $Cc = Co\dfrac{Ro + Ri}{R1\|R2}$. Provide dc feedback from Vo.

8 References

1. Paul R. Gray and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. 2d ed., John Wiley & sons, Inc., 1984.

2. Sergio Franco. *Design with Operational Amplifiers and Analog Integrated Circuits*. McGrawHill, Inc., 1988.

3. Jiri Dostal. *Operational Amplifiers*. Elsevier Scientific Publishing Co., 1981.

8 References

1. Paul R. Gray and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*, 2d ed., John Wiley & sons, Inc., 1984.

2. Sergio Franco. *Design with Operational Amplifiers and Analog Integrated Circuits*, McGraw-Hill, Inc., 1988.

3. Jiri Dostal. *Operational Amplifiers*, Elsevier Scientific Publishing Co., 1981.

Feedback Amplifier Analysis Tools
Application Report

Ronald Mancini

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TEXAS INSTRUMENTS

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Feedback Amplifier Analysis Tools

Ronald Mancini

ABSTRACT

This paper gives the reader a command of the simplest set of tools required to analyze and design feedback amplifiers. These tools are fundamental, and they form the basis of feedback analysis and design.

9 Introduction

Analysis tools have something in common with medicine because they both can be distasteful but necessary. Medicine often tastes bad or has undesirable side effects, and analysis tools involve lots of hard learning work before they can be applied to yield results. Medicine assists the body in fighting an illness; analysis tools assist the brain in learning/designing feedback circuits.

The analysis tools given here are a synopsis of salient points; thus they are detailed enough to get you where you are going without any extras. The references, along with thousands of their counterparts, must be consulted when making an in-depth study of the field. Aspirin, home remedies, and good health practice handle the majority of health problems, and these analysis tools solve the majority of circuit problems.

I have little patience; therefore I would not study these tools in detail prior to reading an application note. A little advanced study however, pays off for those who have patience.

10 Block Diagram Math and Manipulations

Electronic systems and circuits are often represented by block diagrams, and block diagrams have a unique algebra and set of transformations.[1] The block diagrams are used because they are a shorthand pictorial representation of the cause-and-effect relationship between the input and output in a real system. They are a convenient method for characterizing the functional relationships between components. It is not necessary to understand the functional details of a block to manipulate a block diagram.

The input impedance of each block is assumed to be infinite to preclude loading. Also, the output impedance of each block is assumed to be zero to enable high fan-out. The systems designer sets the actual impedance levels, but the fan-out assumption is valid because the block designers adhere to the system designer's specifications. All blocks multiply the input times the block quantity (see Figure 1) unless otherwise specified within the block. The quantity within the block can be a constant as shown in Figure 1(c), or it can be a complex math function involving Laplace transforms. The blocks can perform time-based operations such as differentiation and integration.

INPUT ─── V_O ───○ OUTPUT

(a) Input/Output Impedance

A ──→ Block Description ──→ B

(b) Signal Flow Arrows

A ──→ K ──→ B   B = AK

(c) Block Multiplication

V_I ──→ $\dfrac{d}{dt}$ ──→ $V_O = \dfrac{dV_I}{dt}$

(d) Blocks Perform Functions as Indicated
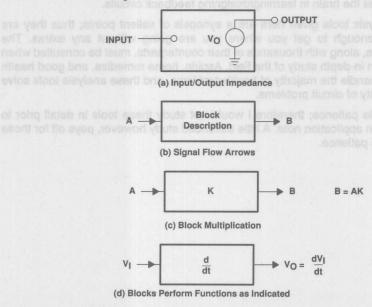
Figure 26. Definition of Blocks

Adding and subtracting are done in special blocks called summing points. Figure 2 gives several examples of summing points. Summing points can have unlimited inputs, can add or subtract, and can have mixed signs yielding addition and subtraction within a single summing point. Figure 3 defines the terms in a typical control system, and Figure 4 defines the terms in a typical electronic feedback system. Multiloop feedback systems (Figure 5) are intimidating, but they can be reduced to a single loop feedback system, as shown in the figure, by writing equations and solving for V_{OUT}/V_{IN}. An easier method for reducing multiloop feedback systems to single loop feedback systems is to follow the rules and use the transforms given in Figure 6.

(a) Additive Summary Point   (b) Subtractive Summary Point   (c) Multiple Input Summary Points
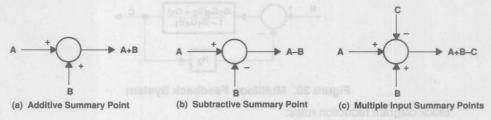
Figure 27. Summary Points
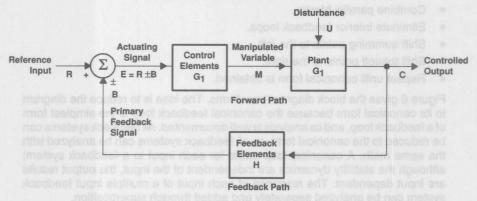
Figure 28. Definition of Control System Terms
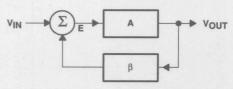
Figure 29. Definition of an Electronic Feedback Circuit
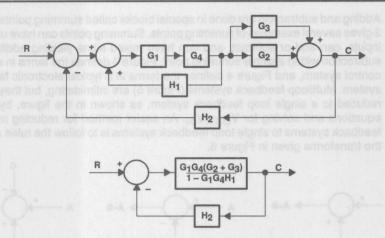
Figure 30. Multiloop Feedback System

Block diagram reduction rules:

- Combine cascade blocks.
- Combine parallel blocks.
- Eliminate interior feedback loops.
- Shift summing points to the left.
- Shift takeoff points to the right.
- Repeat until canonical form is obtained.

Figure 6 gives the block diagram transforms. The idea is to reduce the diagram to its canonical form because the canonical feedback loop is the simplest form of a feedback loop, and its analysis is well documented. All feedback systems can be reduced to the canonical form, so all feedback systems can be analyzed with the same math. A canonical loop exists for each input to a feedback system; although the stability dynamics are independent of the input, the output results are input dependent. The response of each input of a multiple input feedback system can be analyzed separately and added through superposition.
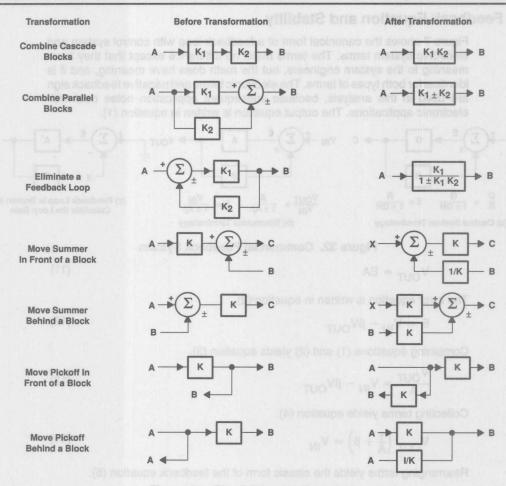
Figure 31. Block Diagram Transforms

11 Feedback Equation and Stability

Figure 7 shows the canonical form of a feedback loop with control system and electronic system terms. The terms make no difference except that they have meaning to the system engineers, but the math does have meaning, and it is identical for both types of terms. The electronic terms and negative feedback sign are used in this analysis, because subsequent application notes deal with electronic applications. The output equation is written in equation (1).

$$\frac{C}{R} = \frac{G}{1 \pm GH} \qquad E = \frac{R}{1 \pm GH}$$

(a) Control System Terminology

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 \pm A\beta} \qquad E = \frac{V_{IN}}{1 \pm A\beta}$$

(b) Electronics Terminology

(c) Feedback Loop is Broken to Calculate the Loop Gain
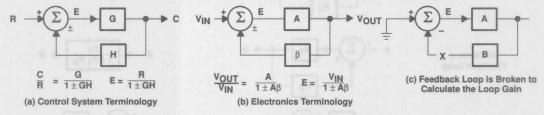
Figure 32. Commercial Feedback System

$$V_{OUT} = EA \tag{11}$$

The error equation is written in equation (2).

$$E = V_{IN} - \beta V_{OUT} \tag{12}$$

Combining equations (1) and (2) yields equation (3).

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \tag{13}$$

Collecting terms yields equation (4).

$$V_{OUT} \left(\frac{1}{A} + \beta \right) = V_{IN} \tag{14}$$

Rearranging terms yields the classic form of the feedback equation (5).

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{15}$$

Notice that when $A\beta$ in equation (5) becomes very large with respect to one the one can be neglected, and equation (5) reduces to equation (6) which is the ideal feedback equation. Under the conditions that $A\beta >> 1$, the system gain is determined by the feedback factor β. Stable passive circuit components are used to implement the feedback factor, thus in the ideal situation, the closed loop gain is predictable and stable because β is stable and predictable.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta} \tag{16}$$

The quantity Aβ is so important that it has been given a special name: loop gain. In Figure 7, when the voltage inputs are grounded (current inputs are opened) and the loop is broken, the calculated gain is the loop gain, Aβ. Now, keep in mind that we are using complex numbers which have magnitude and direction. When the loop gain approaches minus one, or to express it mathematically 1∠180°, equation (5) approaches 1/0 = ∝. The circuit output heads for infinity as fast as it can using the equation of a straight line. If the output were not energy limited, the circuit would explode the world, but happily, it is energy limited, so somewhere it comes up against the limit.

Active devices in electronic circuits exhibit nonlinear phenomena when their output approaches a power supply rail, and the nonlinearity reduces the gain to the point where the loop gain no longer equals 1∠180°. Now the circuit can do two things: first it can become stable at the power supply limit, or second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state where the circuit becomes stable at a power supply limit is named lockup; the circuit will remain in the locked up state until power is removed and reapplied. The second state where the circuit bounces between power supply limits is named oscillatory. Remember, the loop gain, Aβ, is the sole factor determining stability of the circuit or system. Inputs are grounded or disconnected, so they have no bearing on stability. The loop gain criteria is analyzed in depth in the section 6.

Equations (1) and (2) are combined and rearranged to yield equation (7) which gives an indication of the system or circuit error.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{17}$$

First, notice that the error is proportional to the input signal. This is the expected result because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. As the loop gain increases, the error decreases, thus large loop gains are attractive for minimizing errors.

12   Bode Analysis of Feedback Circuits

H. W. Bode developed a quick, accurate, and easy method of analyzing feedback amplifiers, and he published a book about his techniques in 1945.[2] Operational amplifiers had not been developed when Bode published his book, but they fall under the general classification of feedback amplifiers, so they are easily analyzed with Bode techniques. The mathematical manipulations required to analyze a feedback circuit are complicated because they involve multiplication and division. Bode developed the Bode plot which simplifies the analysis through the use of graphical techniques.

The Bode equations are log equations which take the form $20LOG(F(t)) = 20LOG(|F(t)|) +$ phase angle. The terms that are normally multiplied and divided can now be added and subtracted because they are log equations. The addition and subtraction is done graphically, thus easing the calculations and giving the designer a pictorial representation of circuit performance. Equation (8) is written for the low pass filter shown in Figure 8.

Figure 33.   Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + RCs} = \frac{1}{1 + \tau s} \tag{18}$$

Where:

$s = j\omega$, $j = \sqrt{(-1)}$, and $RC = \tau$

The magnitude of this transfer function is $|V_{OUT}/V_{IN}| = 1/\sqrt{(1 + (\tau\omega))^2}$. This magnitude, $|V_{OUT}/V_{IN}| \cong 1$ when $\omega = 0.1/\tau$, it equals 0.707 when $\omega = 1/\tau$, and it is approximately $= 0.1$ when $\omega = 10/\tau$. These points are plotted in Figure 9 using straight line approximations. The negative slope is –20 dB/decade or –6 dB/octave. The magnitude curve is plotted as a horizontal line until it intersects the breakpoint where $\omega = 1/\tau$. The negative slope begins at the breakpoint because the magnitude decreases rapidly at that point. The gain is equal to 1 or 0 dB at very low frequencies, equal to 0.707 or –3 dB at the break frequency, and it keeps falling with a –20 dB/decade slope for higher frequencies.

The phase shift for the low pass filter or any other transfer function is calculated with the aid of equation (9).

$$\phi = \text{tangent}^{-1}\left(\frac{1}{\omega\tau}\right) \tag{19}$$

The phase shift is much harder to approximate because the tangent function is nonlinear. Normally the phase information is only required around the 0 dB intercept point for an active circuit, so the calculations are minimized. The phase is shown in Figure 9, and it is approximated by remembering that the tangent of 90° is 1, and the tangent of 60° is $\sqrt{3}$, and the tangent of 30° is $\sqrt{3}/3$.
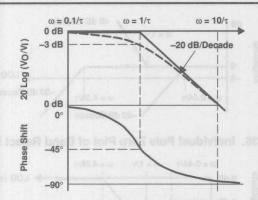
Figure 34. Bode Plot of Low-Pass Filter Transfer Function

A breakpoint occurring in the denominator is called a pole, and it slopes down. Conversely, a breakpoint occurring in the numerator is called a zero, and it slopes up. When the transfer function has multiple poles and zeros, each pole or zero is plotted independently, and the individual poles/zeros are added graphically. If multiple poles, zeros, or a pole/zero combination have the same breakpoint, they are plotted on top of each other. Multiple poles or zeros cause the slope to change by more than 20 dB/decade.

An example of a transfer function with multiple poles and zeros is a band reject filter (see Figure 10). The transfer function of the band reject filter is given in equation (10).
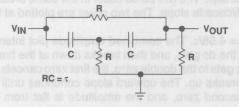
Figure 35. Band Reject Filter

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(1 + \tau s)(1 + \tau s)}{2\left(1 + \frac{\tau s}{0.44}\right)\left(1 + \frac{\tau s}{4.56}\right)} \qquad (20)$$

The pole zero plot for each individual pole and zero is shown in Figure 11, and the combined pole zero plot is shown in Figure 12.
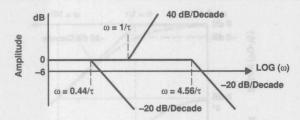
Figure 36. Individual Pole Zero Plot of Band Reject Filter
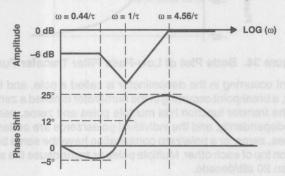
Figure 37. Combined Pole Zero Plot of Band Reject Filter

The individual pole zero plots show the dc gain of 1/2 plotting as a straight line from the –6 dB intercept. The two zeros occur at the same break frequency, thus they have a 40 dB/decade slope. The two poles are plotted at their breakpoints of
$\omega = 0.44/\tau$ and $\omega = 4.56/\tau$. The combined amplitude plot intercepts the axis at –6 dB because of the dc gain, and then breaks down at the first pole. When the amplitude function gets to the double zero, the first zero cancels out the pole, and the second zero breaks up. The upward slope continues until the second pole cancels out the second zero, and the amplitude is flat from that point out in frequency.

When the separation between all the poles and zeros is great, a decade or more in frequency, it is easy to draw the Bode plot. As the poles and zeros get closer the plot gets harder to make. The phase is especially hard to plot because of the tangent function, but picking a few salient points and sketching them in first gets a pretty good approximation.[3] The Bode plot enables the designer to get a good idea of pole zero placement, and it is valuable for fast evaluation of possible compensation techniques. When the situation gets critical, accurate calculations must be made and plotted to get an accurate result.

Consider equation (11).

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{21}$$

Taking the log of equation (11) yields equation (12)

$$20Log\left(\frac{V_{OUT}}{V_{IN}}\right) = 20Log(A) - 20Log(1 + A\beta) \qquad (22)$$

If A and β do not contain any poles or zeros there will be no break points. Then the Bode plot of equation (12) looks like that shown in Figure 13, and because there are no poles to contribute negative phase shift, the circuit cannot oscillate.
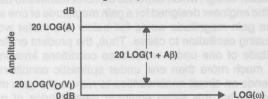
Figure 38. When No Pole Exists in Equation (12)

All real amplifiers have many poles, but they are normally internally compensated so that they appear to have a single pole. Such an amplifier would have an equation similar to that given in equation (13).

$$A = \frac{a}{1 + j\frac{\omega}{\omega_a}} \qquad (23)$$

The plot for the single pole amplifier is shown in Figure 14.
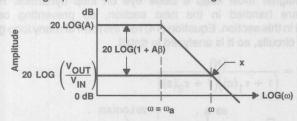
Figure 39. When Equation (12) has a Single Pole

The amplifier gain, A, intercepts the amplitude axis at 20Log(A), and it breaks down at a slope of –20 dB/decade at $\omega = \omega_a$. The negative slope continues for all frequencies greater than the breakpoint, $\omega = \omega_a$. The closed loop circuit gain intercepts the axis at $20Log(V_{OUT}/V_{IN})$, and because β does not have any poles or zeros, it is constant until its projection intersects the amplifier gain at point X. After intersection with the amplifier gain curve, the closed loop gain follows the amplifier gain because the amplifier becomes the controlling factor.

Actually, the closed loop gain starts to roll off earlier, and it is down 3 dB at point X. At point X the difference between the closed loop gain and the amplifier gain is –3 dB, thus according to equation (12) the term $-20Log(1+A\beta) = -3$ dB. The magnitude of 3 dB is $\sqrt{2}$, hence $\sqrt{1 + (A\beta)^2} = \sqrt{2}$, and elimination of the radicals shows that $A\beta = 1$. There is a method [4] of relating phase shift and stability to the slope of the closed loop gain curves, but only the Bode method is covered here. An excellent discussion of poles, zeros, and their interaction is given by M. E Van Valkenberg,[5] and he also includes some excellent prose to liven the discussion.

13 Loop Gain Plots are the Key to Understanding Stability

Stability is determined by the loop gain, and when $A\beta = -1 = |1| \angle 180°$ instability or oscillation occurs. If the magnitude of the gain exceeds one, it is usually reduced to one by circuit nonlinearities, so oscillation generally results for situations where the gain magnitude exceeds one.

Consider oscillator design which depends on nonlinearities to decrease the gain magnitude; if the engineer designed for a gain magnitude of one at nominal circuit conditions, the gain magnitude would fall below one under worst case circuit conditions causing oscillation to cease. Thus, the prudent engineer designs for a gain magnitude of one under worst case conditions knowing that the gain magnitude is much more than one under optimistic conditions. The prudent engineer depends on circuit nonlinearities to reduce the gain magnitude to the appropriate value, but this same engineer pays a price of poorer distortion performance. Sometimes a design compromise is reached by putting a nonlinear component, such as a lamp, in the feedback loop to control the gain without introducing distortion.

Some high gain control systems always have a gain magnitude greater than one, but they avoid oscillation by manipulating the phase shift. The amplifier designer who pushes the amplifier for superior frequency performance has to be careful not to let the loop gain phase shift accumulate to 180°. Problems with overshoot and ringing pop up before the loop gain reaches 180° phase shift, thus the amplifier designer must keep a close eye on loop dynamics. Ringing and overshoot are handled in the next section, so preventing oscillation is emphasized in this section. Equation (14) has the form of many loop gain transfer functions or circuits, so it is analyzed in detail.

$$(A)\beta = \frac{(K)}{\left(1 + \tau_1(s)\right)\left(1 + \tau_2(s)\right)} \tag{24}$$
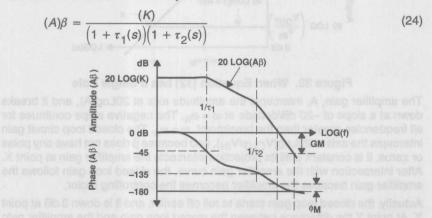
Figure 40. Magnitude and Phase Plot of Equation (14)

The quantity, K, is the dc gain, and it plots as a straight line with an intercept of 20Log(K). The Bode plot of equation (14) is shown in Figure 15. The two break points, $\omega = \omega_1 = 1/\tau_1$ and $\omega = \omega_2 = 1/\tau_2$, are plotted in the Bode plot. Each breakpoint adds −20 dB/decade slope to the plot, and 45° phase shift accumulates at each breakpoint. This transfer function is referred to as a two slope because of the two breakpoints. The slope of the curve when it crosses the 0 dB intercept indicates phase shift and the ability to oscillate. Notice that a one slope can only accumulate 90° phase shift, so when a transfer function passes through 0 dB with a one slope, it cannot oscillate. Furthermore, a two-slope system can accumulate 180° phase shift, therefore a transfer function with a two or greater slope is capable of oscillation.

A one slope crossing the 0 dB intercept is stable, whereas a two or greater slope crossing the 0 dB intercept may be stable or unstable depending upon the accumulated phase shift. Figure 15 defines two stability terms; the phase margin, ϕ_M, and the gain margin, G_M. Of these two terms the phase margin is much more popular because phase shift is critical for stability. Phase margin is a measure of the difference in the actual phase shift and the theoretical 180° required for oscillation, and the phase margin measurement or calculation is made at the 0 dB crossover point. The gain margin is measured or calculated at the 180° phase crossover point. Phase margin is expressed mathematically in equation (15).

$$\phi_M = 180 - \tan^{-1}(A\beta) \qquad (25)$$

The phase margin in Figure 15 is very small, 20°, so it is hard to measure or predict from the Bode plot. A designer probably doesn't want a 20° phase margin because the system overshoots and rings badly, but this case points out the need to calculate small phase margins carefully. The circuit is stable, and it does not oscillate because the phase margin is positive. Also, the circuit with the smallest phase margin has the highest frequency response and bandwidth.
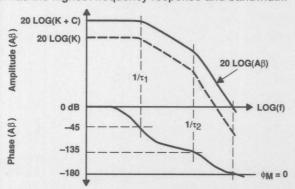
Figure 41. Magnitude and Phase Plot of the Loop Gain Increased to (K+C)

Increasing the loop gain to (K+C) as shown in Figure 16 shifts the magnitude plot up. If the pole locations are kept constant, the phase margin reduces to zero as shown, and the circuit will oscillate. The circuit is not good for much in this condition because production tolerances and worst case conditions insure that the circuit will oscillate when you want it to amplify, and vice versa.
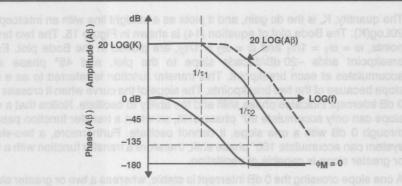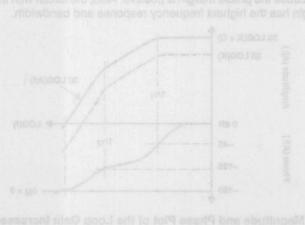
Figure 42. Magnitude and Phase Plot of the Loop Gain With Pole Spacing Reduced

The circuit poles are spaced closer in Figure 17, and this results in a faster accumulation of phase shift. The phase margin is zero because the loop gain phase shift reaches 180° before the magnitude passes through 0 dB. This circuit oscillates, but it is not a very stable oscillator because the transition to 180° phase shift is very slow. Stable oscillators have a very sharp transition through 180°.

When the closed loop gain is increased the feedback factor, β, is decreased because $V_{OUT}/V_{IN} = 1/β$ for the ideal case. This in turn decreases the loop gain, Aβ, thus the stability increases. In other words, increasing the closed loop gain makes the circuit more stable. Stability is not important except to oscillator designers because overshoot and ringing become intolerable to linear amplifiers long before oscillation occurs. The overshoot and ringing situation is investigated in the next section.

14 The Second Order Equation and Ringing/Overshoot Predictions

The second order equation is a common approximation used for feedback system analysis because it describes a two-pole circuit which is the most common approximation used. All real circuits are more complex than two poles, but except for a small fraction, they can be represented by a two-pole equivalent. The second order equation is extensively described in electronic and control literature[6].

$$(1 + A\beta) = 1 + \frac{K}{\left(1 + \tau_1 s\right)\left(1 + \tau_2 s\right)} \tag{26}$$

After algebraic manipulation equation (16) is presented in the form of equation (17).

$$s^2 + \frac{\tau_1 + \tau_2}{\tau_1 \tau_2} + \frac{1 + K}{\tau_1 \tau_2} = 0 \tag{27}$$

Equation (17) is compared to the second order control equation (18), and the damping ratio, z, and natural frequency, w_N are obtained through like term comparisons.

$$s^2 + 2\xi\omega_N s + \omega_N^2 \tag{28}$$

Comparing these equations yields formulas for the phase margin and per cent overshoot as a function of damping ratio.

$$\omega_N = \sqrt{\frac{1 + K}{\tau_1 \tau_2}} \tag{29}$$

$$\xi = \frac{\tau_1 + \tau_2}{2\omega_N \tau_1 \tau_2} \tag{30}$$

When the two poles are well separated, equation (21) is valid.

$$\phi_M = \text{tangent}^{-1}(2\xi) \tag{31}$$

The salient equations are plotted in Figure 18 which enables a designer to determine the phase margin and overshoot when the gain and pole locations are known.
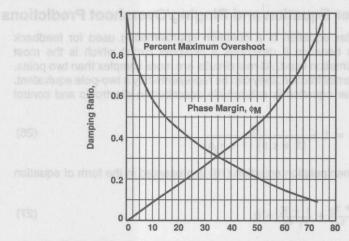
Figure 43. Phase Margin and Overshoot vs Damping Ratio

Enter Figure 18 at the calculated damping ratio, say 0.4, and read the overshoot at 25% and the phase margin at 42°. If a designer had a circuit specification of 5% maximum overshoot, then the damping ratio must be 0.78 with a phase margin of 62°.

15 Summary

These equations and examples are adequate to get designers started in the design and analysis of feedback circuits. When the engineers reach the point where the examples and equations given here are inadequate, they must go to the references for more information. If the engineers find themselves digging through the references on a regular basis, they should consider becoming analog design engineers.

16 References

1. DiStefano, Stubberud, and Williams, *Theory and Problems of Feedback and Control Systems, Schaum's Outline Series*, Mc Graw Hill Book Company, 1967

2. Bode, H. W., Network *Analysis And Feedback Amplifier Design*, D. Van Nostrand, Inc., 1945

3. Frederickson, Thomas, *Intuitive Operational Amplifiers*, McGraw Hill Book Company, 1988

4. Bower, J. L. and Schultheis, P. M., *Introduction To The Design Of Servomechanisms*, Wiley, 1961

5. Van Valkenberg, M. E., *Network Analysis*, Prentice-Hall, 1964

6. Del Toro, V., and Parker, S., Principles of Control Systems Engineering, McGraw–Hill, 1960.

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Noise Analysis in Operational Amplifier Circuits

Application Report

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Noise Analysis in Operational Amplifier Circuits

ABSTRACT

This application report uses standard circuit theory and noise models to calculate noise in op amp circuits. Example analysis of the inverting, noninverting, and differential-amplifier circuits shows how calculations are performed. Characteristics of noise sources are presented to help the designer make informed decisions when designing for noise.

Introduction

"Statistical fluctuation of electric charge exists in all conductors, producing random variation of potential between the ends of the conductor. The electric charges in a conductor are found to be in a state of thermal agitation, in thermodynamic equilibrium with the heat motion of the atoms of the conductor. The manifestation of the phenomenon is a fluctuation of potential difference between the terminals of the conductor" – J.B. Johnson[1]

"The term spontaneous fluctuations, although, perhaps, theoretically the most appropriate, is not commonly used in practice; usually it is simply called noise" – Aldert van der Ziel[2]

Early investigators of noise likened spontaneous fluctuations of current and voltage in electric circuits to Brownian motion. In 1928 Johnson[1] showed that electrical noise was a significant problem for electrical engineers designing sensitive amplifiers. The limit to the sensitivity of an electrical circuit is set by the point at which the signal-to-noise ratio drops below acceptable limits.

Notational Conventions

In the calculations throughout this report, lower case letters e and i indicate independent voltage and current noise sources; upper case letters E and I indicate combinations or amplified versions of the independent sources.

Spectral Density

A spectral density is a noise voltage or noise current per root hertz, i.e. $V\sqrt{Hz}$ or $A\sqrt{Hz}$. Spectral densities are commonly used to specify noise parameters. The characteristic equations that identify noise sources are always integrated over frequency, indicating that spectral density is the natural form for expressing noise sources. To avoid confusion in the following analyses, spectral densities are identified, when used, by stating them as volts or amps per root hertz.

Types of Noise

In electrical circuits there are 5 common noise sources:

- Shot noise
- Thermal noise
- Flicker noise
- Burst noise
- Avalanche noise

In op amp circuits, burst noise and avalanche noise are normally not problems, or they can be eliminated if present. They are mentioned here for completeness, but are not considered in the noise analysis.

Shot Noise

Shot noise is always associated with current flow. Shot noise results whenever charges cross a potential barrier, like a pn junction. Crossing the potential barrier is a purely random event. Thus the instantaneous current, i, is composed of a large number of random, independent current pulses with an average value, i_D. Shot noise is generally specified in terms of its mean-square variation about the average value. This is written as $\overline{i_n^2}$, where :

$$\overline{i_n^2} = \overline{(i - i_D)^2} = \int 2qi_D df \qquad (32)$$

Where q is the electron charge (1.62×10^{-19} C) and df is differential frequency.

Shot noise is spectrally flat or has a uniform power density, meaning that when plotted vs. frequency, it has a constant value. Shot noise is independent of temperature.

The term qi_D is a current power density having units A^2/Hz.

Thermal Noise

Thermal noise is caused by the thermal agitation of charge carriers (electrons or holes) in a conductor. This noise is present in all passive resistive elements.

Like shot noise, thermal noise is spectrally flat or has a uniform power density, but thermal noise is independent of current flow.

Thermal noise in a conductor can be modeled as voltage, or current. When modeled as a voltage it is placed in series with an otherwise noiseless resistor. When modeled as a current it is placed in parallel with an otherwise noiseless resistor. The average mean-square value of the voltage noise source or current noise source is calculated by:

$$\overline{e^2} = \int 4kTR df \text{ or } \overline{i^2} = \int (4kT / R) df \qquad (33)$$

Where k is Boltzmann's constant (1.38×10^{-23} j/K), T is absolute temperature in Kelvin (K), R is the resistance of the conductor in ohms (Ω) and df is differential frequency.

The terms *4kTR* and *4kT/R* are voltage and current power densities having units of V^2/Hz and A^2/Hz.

Flicker Noise

Flicker noise is also called *1/f* noise. It is present in all active devices and has various origins. Flicker noise is always associated with a dc current, and its average mean-square value is of the form:

$$\overline{e^2} = \int \left(K_e^2 / f \right) df \text{ or } \overline{i^2} = \int \left(K_i^2 / f \right) df$$

(34)

Where K_e and K_i are the appropriate device constants (in volts or amps), *f* is frequency, and *df* is differential frequency.

Flicker noise is also found in carbon composition resistors where it is often referred to as excess noise because it appears in addition to the thermal noise. Other types of resistors also exhibit flicker noise to varying degrees, with wire wound showing the least. Since flicker noise is proportional to the dc current in the device, if the current is kept low enough, thermal noise will predominate and the type of resistor used will not change the noise in the circuit.

The terms K_e^2/f and K_i^2/f are voltage and current power densities having units of V^2/Hz and A^2/Hz.

Burst Noise

Burst noise, also called popcorn noise, appears to be related to imperfections in semiconductor material and heavy ion implants. Burst noise makes a popping sound at rates below 100 Hz when played through a speaker. Low burst noise is achieved by using clean device processing.

Avalanche Noise

Avalanche noise is created when a pn junction is operated in the reverse breakdown mode. Under the influence of a strong reverse electric field within the junction's depletion region, electrons have enough kinetic energy that, when they collide with the atoms of the crystal lattice, additional electron-hole pairs are formed. These collisions are purely random and produce random current pulses similar to shot noise, but much more intense.

Noise Characteristics

Since noise sources have amplitudes that vary randomly with time, they can only be specified by a probability density function. Thermal noise and shot noise have Gaussian probability density functions. The other forms of noise noted do not. If δ is the standard deviation of the Gaussian distribution, then the instantaneous value lies between the average value of the signal and $\pm\delta$ 68% of the time. By definition, δ^2 (variance) is the average mean-square variation about the average value. This means that in noise signals having Gaussian distributions of amplitude, the average mean-square variation about the average value, $\overline{i^2}$ or $\overline{e^2}$, is the variance δ^2, and the rms value is the standard deviation δ.

Theoretically the noise amplitude can have values approaching infinity. However, the probability falls off rapidly as amplitude increases. An effective limit is $\pm3\delta$, since the noise amplitude is within these limits 99.7% of the time. Figure 1 shows graphically how the probability of the amplitude relates to the rms value.
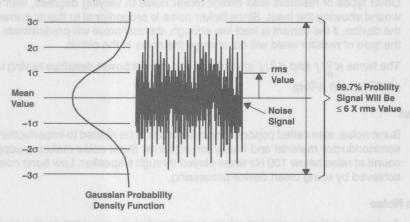
Figure 44. Gaussian Distribution of Noise Amplitude

Since the rms value of a noise source is equal to δ, to assure that a signal is within peak-to-peak limits 99.7% of the time, multiply the rms value by 6($+3\delta$–(-3δ)): $Erms \times 6 = Epp$. For more or less assurance, use values between 4(95.4%) and 6.8(99.94%).

Adding Noise Sources

With multiple noise sources in a circuit, the signals must be combined properly to obtain the overall noise signal.

Consider the example of two resistors, R_1 and R_2, connected in series. Each resistor has a noise generator associated with it as shown in Figure 2 where

$$\overline{e_1^2} = \int 4kTR_1\,df \quad and \quad \overline{e_2^2} = \int 4kTR_2\,df.$$

Figure 45. R1 and R2 Noise Model

To calculate the average mean square voltage, $\overline{E_t^2}$, across the two resistors, let

$E_t(t) = e_1(t) + e_2(t)$ be the instantaneous values. Then

$$\overline{E_t\,(t)^2} = \overline{\left[e_1(t) + e_2(t)\right]^2} = \overline{e_1(t)^2} + \overline{e_2(t)^2} + \overline{2e_1(t)e_2(t)} \tag{35}$$

Since the noise voltages, $e_1(t)$ and $e_2(t)$, arise from separate resistors, they are independent, and the average of their product is zero:

$$\overline{2e_1(t)e_2(t)} = 0 \tag{36}$$

This results in

$$\overline{E_t^2} = \overline{e_1^2} + \overline{e_2^2}. \tag{37}$$

Therefore, as long as the noise sources arise from separate mechanisms and are independent, which is usually the case, the average mean square value of a sum of separate independent noise sources is the sum of the individual average mean square values. Thus in our example $\overline{E_t^2} = \int 4kT(R_1 + R_2)df$, which is what would be expected. This is derived using voltage sources, but also is true for current sources. The same result can be shown to be true when considering two independent sine wave sources.

Noise Spectra

A pure sine wave has power at only one frequency. Noise power, on the other hand, is spread over the frequency spectrum. Voltage noise power density, $\overline{e^2}/Hz$, and current noise power density, $\overline{i^2}/Hz$ are often used in noise calculations. To calculate the mean-square value, the power density is integrated over the frequency of operation. This application report deals with noise that is constant over frequency, and noise that is proportional to 1/f.

Spectrally flat noise is referred to as white noise. When plotted vs frequency, white noise is a horizontal line of constant value.

Flicker noise is 1/f noise and is stated in equation form as:

$$\overline{e^2} = \int \left(K_e^2/f \right)df \ \ or \ \ \overline{i^2} = \int \left(K_i^2/f \right)df$$

See equation (3). When plotted vs frequency on log-log scales, 1/f noise is a line with constant slope. If the power density V^2/Hz is plotted, the slope is –1 decade per decade. If the square root of the power density, $V_{rms}/\sqrt{Hz}$, is plotted, the slope is –0.5 decade per decade.

Figure 3 shows the spectra of 1/f and white noise per root hertz.
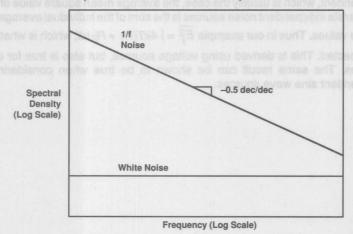
Figure 46. 1/f and White Noise Spectra

Integrating Noise

To determine the noise or current voltage over a given frequency band, the beginning and ending frequencies are used as the *f* integration limits and the integral evaluated. The following analysis uses voltages; the same is true for currents.

Given a white or constant voltage noise vs frequency source then:

$$\overline{e^2} = \int_{f_L}^{f_H} C \, df = C \left(f_H - f_L \right) \tag{38}$$

where $\overline{e^2}$ is the average mean-square voltage, C is the spectral power density per hertz (constant), f_L is the lowest frequency, and f_H is the highest frequency.

Given a 1/f voltage noise vs. frequency source then:

$$\overline{e^2} = \int_{f_L}^{f_H} \frac{K^2}{f} \, df = K^2 \ln \frac{f_H}{f_L} \tag{39}$$

where $\overline{e^2}$ is the average mean-square voltage, K is the appropriate device constant in volts, f_L is the lowest frequency, and f_H is the highest frequency.

The input noise of an op amp contains both 1/f noise and white noise. The point in the frequency spectrum where 1/f noise and white noise are equal is referred to as the noise corner frequency, f_{nc}. Using the same notation as in the equations above, this means that $K^2/f_{nc} = C$. It is useful to find f_{nc} because the total average mean-square noise can be calculated by adding equations (7) and (8) and substituting Cf_{nc} for K^2:

$$\overline{E^2} = C \left(f_{nc} \ln \frac{f_H}{f_L} + f_H - f_L \right) \tag{40}$$

Where C is the square of the white noise voltage specification for the op amp.

Figure 4 shows the equivalent input noise voltage vs frequency graph for the TLV2772 as normally displayed in the data sheet.

f_{nc} can be determined visually from the graph of equivalent input noise per root hertz vs. frequency graph that is included in most op amp data sheets. Since at f_{nc} the white noise and 1/f noise are equal, f_{nc} is the frequency at which the noise is $\sqrt{2} \times$ white noise specification. This would be about *17 nV/√Hz* for the TLV2772, which is at 1000 Hz as shown in Figure 4.

Another way to find f_{nc}, is to determine K^2 by finding the equivalent input noise voltage per root hertz at the lowest possible frequency in the 1/f noise region, square this value, subtract the white noise voltage squared, and multiply by the frequency. Then divide K^2 by the white noise specification squared. The answer is f_{nc}.

For example, the TLV2772 has a typical noise voltage of *130 nV/√Hz* at 10 Hz.

The typical white noise specification for the TLV2772 is 12 *nV/√Hz*

$$K^2 = \left[\left(130 \ nV/\sqrt{Hz} \right)^2 - \left(12 \ nV/\sqrt{Hz} \right)^2 \right] \times (10 \ Hz) = 167560 \ (nV)^2$$

Therefore, $f_{nc} = (167560 (nV)^2)/(144(nV)^2/Hz) = 1163$ Hz
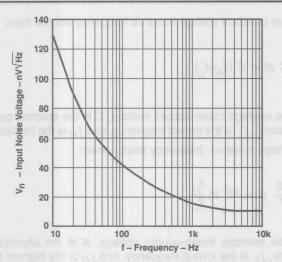
Figure 47. Equivalent Input Noise Voltage vs. Frequency for TLV2772 as Normally Presented

Figure 5 was constructed by interpreting the equivalent input noise voltage vs frequency graph for the TLV2772 and plotting the values on log-log scales. The –0.5 dec/dec straight line nature of 1/f noise when plotted on log-log scales can be seen.
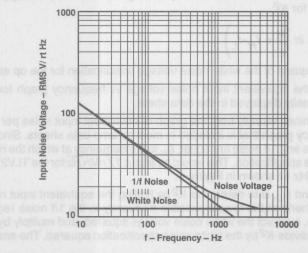
Figure 48. Equivalent Input Noise Voltage vs. Frequency for TLV2772 on Log-Log Scale

Equivalent Noise Bandwidth

Equations (7), (8), and (9) are only true if the bandwidth If the op amp circuit is brick-wall. In reality there is always a certain amount of out-of-band energy transferred. The equivalent noise bandwidth (ENB) is used to account for the extra noise so that brick-wall frequency limits can be used in equations (7), (8), and (9). Figure 6 shows the idea for a first order low-pass filter.
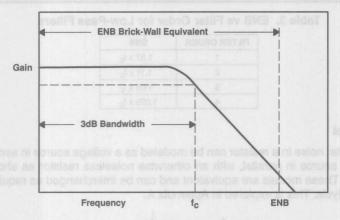
Figure 49. ENB Brick-wall Equivalent

Figure 7 shows and example of a simple RC filter used to filter a voltage noise source, e_{in}.

$$A_{n(f)} = \frac{1}{1 + jwRC} \Rightarrow \left|A_{n(f)}\right|^2 = \frac{1}{1 + (wRC)^2}$$

Figure 50. RC Filter

$A_{n(f)}$ is the frequency-dependant gain of the circuit, and e_{on} is calculated:

$$e_{on} = \sqrt{\int_0^\infty \left|A_{n(f)}\right|^2 e_{in}^2 \, df} \tag{41}$$

Assuming e_{in} is a white noise source (specified as a spectral density in $V/\sqrt{Hz}$), using radian measure for frequency, and substituting for $A_{n(f)}$, the equation can be solved as follows:

(42)

$$e_{on} = e_{in} \sqrt{\int_0^\infty \frac{1}{1 + (\omega RC)^2} \, d\omega} = e_{in} \sqrt{\frac{1}{RC} \left| tan^{-1} \omega RC \right|_0^\infty} = e_{in} \sqrt{\frac{1}{RC} \frac{\Pi}{2}}$$

So that the ENB = 1.57 x 3dB bandwidth in this first-order system. This result holds for any first-order low-pass function. For higher order filters the ENB approaches the normal cutoff frequency, f_c, of the filter. Table 1 shows the ENB for different order low-pass filters.

Table 3. ENB vs Filter Order for Low-Pass Filters

FILTER ORDER	ENB
1	$1.57 \times f_C$
2	$1.11 \times f_C$
3	$1.05 \times f_C$
4	$1.025 \times f_C$

Resistor Noise Model

To reiterate, noise in a resistor can be modeled as a voltage source in series, or a current source in parallel, with an otherwise noiseless resistor as shown in Figure 8. These models are equivalent and can be interchanged as required to ease analysis. This is explored in Appendix A.

$$\overline{i^2} = \int \frac{4kT}{R} df \qquad \overline{e^2} = \int 4\ kTR\ df$$

Figure 51. Resistor Noise Models

Op Amp Circuit Noise Model

Op amp manufacturers measure the noise characteristics for a large sampling of a device. This information is compiled and used to determine the typical noise performance of the device. The noise specifications published by Texas Instruments in their data sheets refer the measured noise to the input of the op amp. The part of the internally generated noise that can properly be represented by a voltage source is placed in series with the positive input to an otherwise noiseless op amp. The part of the internally generated noise that can properly be represented by current sources is placed between each input and ground in an otherwise noiseless op amp. Figure 9 shows the resulting noise model for a typical op amp.
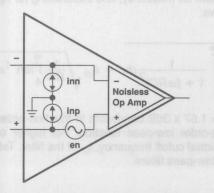
Figure 52. Op Amp Noise Model

Inverting and Non-Inverting Op Amp Circuit Noise Calculations

To perform a noise analysis, the foregoing noise models are added to the circuit schematic and the input signal sources are shorted to ground. When this is done to either an inverting or a noninverting op amp circuit, the same circuit results, as shown in Figure 10. This circuit is used for the following noise analysis.
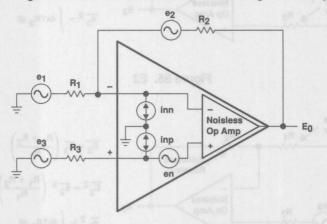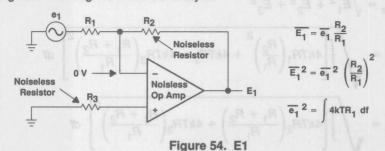
Figure 53. Inverting and Non-Inverting Noise Analysis Circuit

At first, this analysis may appear somewhat daunting, but it can be deciphered piece by piece. Using the principles of superposition, each of the noise sources is isolated, and everything else is assumed to be noiseless. Then the results can be added according to the rules for adding independent noise sources. An ideal op amp is assumed for the noiseless op amp. In the end it will all seem simple, if a little tedious the first time through.

Figures 11 through 13 show the analysis.
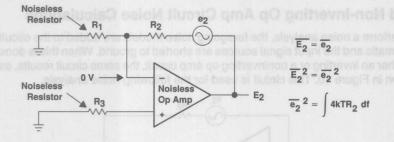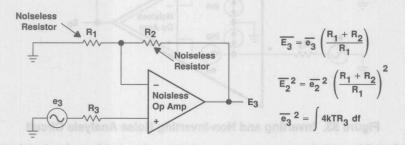
$$\overline{E_1} = \overline{e_1} \frac{R_2}{R_1}$$

$$\overline{E_1}^2 = \overline{e_1}^2 \left(\frac{R_2}{R_1}\right)^2$$

$$\overline{e_1}^2 = \int 4kTR_1 \, df$$

Figure 54. E1

Figure 55. E2

$$\overline{E_2} = \overline{e_2}$$

$$\overline{E_2}^2 = \overline{e_2}^2$$

$$\overline{e_2}^2 = \int 4kTR_2\ df$$

Figure 56. E3

$$\overline{E_3} = \overline{e_3}\left(\frac{R_1 + R_2}{R_1}\right)$$

$$\overline{E_2}^2 = \overline{e_2}^2\left(\frac{R_1 + R_2}{R_1}\right)^2$$

$$\overline{e_3}^2 = \int 4kTR_3\ df$$

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{Rrms}, due to the thermal noise of the resistors in the circuit:

(43)

$$E_{Rrms} = \sqrt{\overline{E_1}^2 + \overline{E_2}^2 + \overline{E_3}^2}$$

$$E_{Rrms} = \sqrt{\int\left[4kTR_1\left(\frac{R_2}{R_1}\right)^2 + 4kTR_2 + 4kTR_3\left(\frac{R_1 + R_2}{R_1}\right)^2\right]df}$$

$$E_{Rrms} = \sqrt{\int\left[4kTR_2\left(\frac{R_1 + R_2}{R_1}\right) + 4kTR_3\left(\frac{R_1 + R_2}{R_1}\right)^2\right]df}$$

If it is desired to know the resistor noise referenced to the input, E_{iRrms}, the output noise is divided by the noise gain, A_n, of the circuit:

$$A_n = \left(\frac{R_1 + R_2}{R_1}\right)$$

(44)

$$(45)$$

$$E_{iRrms}^2 = \left(\frac{E_{Rrms}}{A_n}\right)^2 = \int \frac{\left[4kTR_2\left(\frac{R_1+R_2}{R_1}\right) + 4kTR_3\left(\frac{R_1+R_2}{R_1}\right)^2\right]df}{\left(\frac{R_1+R_2}{R1}\right)^2} = \int 4kT\left[\left(\frac{R_1R_2}{R_1+R_2}\right) + R_3\right]df$$

Normally R_3 is chosen to be equal to the parallel combination of R_1 and R_2 to minimize offset voltages due to input bias current. If this is done, the equation simplifies to:

$$(46)$$

$$E_{iRrms} = \sqrt{\int 8kTR_3 \; df} \qquad When \; R3 = \left(\frac{R_1R_2}{R_1+R_2}\right)$$

Now consider the noise sources associated with the op amp itself. The analysis proceeds as before as shown in Figures 14 through 16.

Figure 57. E_p

$$\overline{E_p^2} = \int\left[(e_p)\left(\frac{R_1+R_2}{R_1}\right)\right]^2 df$$

Figure 58. E_{np}

$$\overline{E_{np}^2} = \int\left[(i_{np})(R_3)\left(\frac{R_1+R_2}{R_1}\right)\right]^2 df$$

$$\overline{E_{nn}}^2 = \int \left[(i_{nn})(R_2) \right]^2 df$$
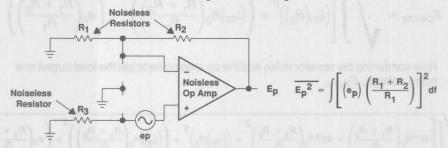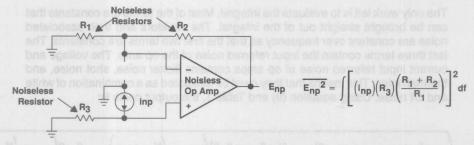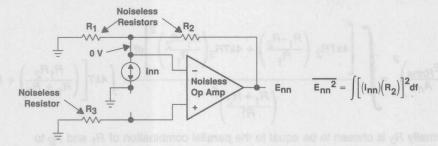
Figure 59. E_{nn}

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{oarms}, due to the input referred op amp noise in the circuit:

$$E_{oarms} = \sqrt{\overline{E_p}^2 + \overline{E_{np}}^2 + \overline{E_{nn}}^2}$$

(47)

$$E_{oarms} = \sqrt{\int\int \left[\left(i_{nn}(R_2) \right)^2 + \left((i_{np})R_3 \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 + \left(e_p \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 \right] df}$$

Now combining the resistor noise and the op amp noise to get the total output rms noise voltage, E_{Trms}.

(48)

$$E_{Trms} = \sqrt{\int\int \left[4kTR_2 \left(\frac{R_1 + R_2}{R_1} \right) + 4kTR_3 \left(\frac{R_1 + R_2}{R_1} \right)^2 + \left((i_{np})R_2 \right)^2 + \left((i_{np})R_3 \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 + \left(e_n \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 \right] df}$$

The only work left is to evaluate the integral. Most of the terms are constants that can be brought straight out of the integral. The resistors and their associated noise are constant over frequency so that the first two terms are constants. The last three terms contain the input referred noise of the op amp. The voltage and current input referred noise of op amps contains flicker noise, shot noise, and thermal noise. This means that they must be evaluated as a combination of white and 1/f noise. Using equation (9) and Table 1, the output noise is:

$$E_{Trms} = \sqrt{ ENB \left(4kTR_2 A + 4kTR_3 A^2 \right) + i_w^2 \left(R_2^2 + R_3^2 A^2 \right) \left(f_{inc} \ln \frac{f_H}{f_L} + ENB \right) + e_w^2 A^2 \left(f_{enc} \ln \frac{f_H}{f_L} + ENB \right)}$$

Where $A = (R_1 + R_2)/R_1$, i_w is the white current noise specification (spectral density in $A/\sqrt{Hz}$), f_{inc} is the current noise corner frequency, e_w is the white voltage noise specification (spectral density in $V/\sqrt{Hz}$, and f_{enc} is the voltage noise corner frequency. ENB is determined by the frequency characteristics of the circuit. f_H/f_L is set equal to ENB.

In CMOS input op amps, noise currents are normally so low that the input noise voltage dominates and the i_w terms are not factored into the noise computation. Also, since bias current is very low, there is no need to use R_3 for bias current compensation, and it, too, is removed from the circuit and the calculations. With these simplifications the formula above reduces to:

$$E_{Trms} = \sqrt{ENB\ 4kTR_2\ A + e_w^2\ A^2\left(f_{enc}\ ln\frac{f_H}{f_L} + ENB\right)}$$ CMOS input op amps

Differential Op Amp Circuit Noise Calculations

A noise analysis for a differential amplifier can be done in the same manner as the previous example. Figure 17 shows the circuit used for the analysis.
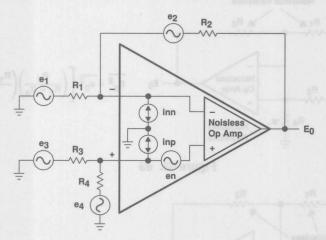
Figure 60. Differenital Op Amp Circuit Noise Model

Figures 18 through 21 show the analysis.
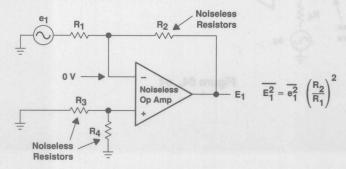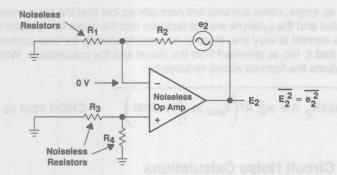
$$\overline{E_1^2} = \overline{e_1^2}\left(\frac{R_2}{R_1}\right)^2$$

Figure 61. e1

Figure 62. e2
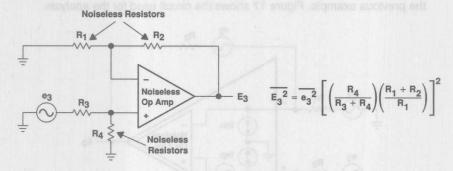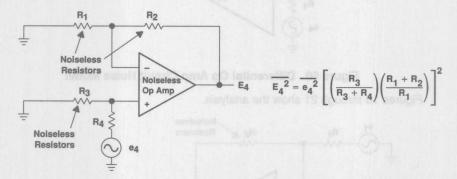
$$\overline{E_2^2} = \overline{e_2^2}$$

Figure 63. e3

$$\overline{E_3^2} = \overline{e_3^2}\left[\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right)\right]^2$$

Figure 64. e4

$$\overline{E_4^2} = \overline{e_4^2}\left[\left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right)\right]^2$$

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{Rrms}, due to the thermal noise in the resistors in the circuit:

(49)

$$E_{Rrms} = \sqrt{E1^2 + E2^2 + E3^2 + E4^2}$$

$$E_{Rrms} = \sqrt{\iint \left[\left(4kTR1\left(\frac{R2}{R1}\right)^2 \right) + (4kTR2) + \left(4kTR3\left(\frac{R4}{R3+R4}\right)^2 \left(\frac{R1+R2}{R1}\right)^2 \right) + \left(4kTR4\left(\frac{R3}{R3+R4}\right)^2 \left(\frac{R1+R2}{R1}\right)^2 \right) \right] df}$$

$$E_{Rrms} = \sqrt{\int 4kT \left[\frac{R2^2}{R1} + R2 + \left(R3\left(\frac{R4}{R3+R4}\right)^2 \left(\frac{R1+R2}{R1}\right)^2 \right) + \left(R4\left(\frac{R4}{R3+R4}\right)^2 \left(\frac{R1+R2}{R1}\right)^2 \right) \right] df}$$

Normally $R_1 = R_3$ and $R_2 = R_4$. Making this substitution reduces the above equation to:

$$E_{Rrms} = \sqrt{\int 8kTR2\left(1 + \frac{R2}{R1}\right) df} \qquad \text{If } R1 = R3 \text{ and } R2 = R4 \tag{50}$$

Now consider the noise sources associated with the op amp itself. The analysis proceeds as before as shown in Figures 22 through 24.

$$\overline{Enp^2} = \int \left[(Inp)\left(\frac{R3R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) \right]^2 df$$

Figure 65. inp

$$\overline{Ep^2} = \int \left[(ep)\left(\frac{R1+R2}{R1}\right) \right]^2 df$$
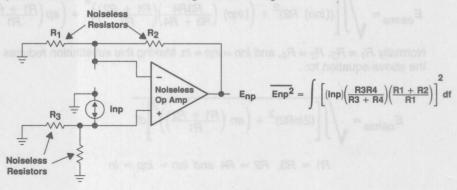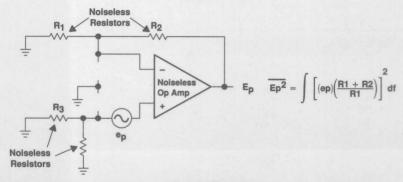
Figure 66. ep
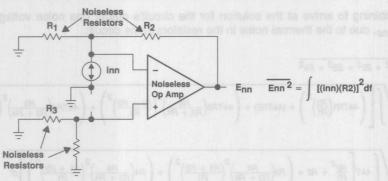
Figure 67. inn

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{oarms}, due to the input referred op amp noise in the circuit:

$$E_{oarms} = \sqrt{\overline{Ep}^2 + \overline{Enp}^2 + \overline{Enn}^2} \tag{51}$$

$$E_{oarms} = \sqrt{\iint \left[((inn)\ R2)^2 + \left((inp) \left(\frac{R3R4}{R3 + R4} \right) \left(\frac{R1 + R2}{R1} \right) \right)^2 + \left(ep \left(\frac{R1 + R2}{R1} \right) \right)^2 \right] df}$$

Normally $R_1 = R_3$, $R_2 = R_4$, and $inn = inp = in$. Making this substitution reduces the above equation to:

$$E_{oarms} = \sqrt{\iint \left[(2inR2)^2 + \left(en \left(\frac{R1 + R2}{R1} \right) \right)^2 \right] df} \tag{52}$$

$$R1 = R3, \ \ R2 = R4 \ \ and \ \ inn = inp = in$$

Now combine the resistor noise and the op amp noise to get the total output rms noise voltage, E_{Trms}.

(53)

$$E_{Trms} = \sqrt{\iint \left[\left((inn)\ R2\right)^2 + \left((inp)\left(\frac{R3R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right)\right)^2 + \left(en\left(\frac{R1+R2}{R1}\right)\right)^2 + \left(4kTR1\left(\frac{R2}{R1}\right)^2\right) \right.}$$
$$\overline{\left. + (4kTR2) + \left(4kTR3\left(\frac{R4}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right) + \left(4kTR4\left(\frac{R3}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right) \right] df}$$

$$E_{Trms} = \sqrt{\iint \left[\left((inn)\ R2\right)^2 + \left((inp)\left(\frac{R3R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right)\right)^2 + \left(en\left(\frac{R1+R2}{R1}\right)\right)^2 \right.}$$
$$\overline{\left. + 4kT\left[\frac{R2^2}{R1} + R2 + \left(R3\left(\frac{R4}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right) + \left(R4\left(\frac{R4}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right)\right] \right] df}$$

Substituting $R_1 = R_3$, $R_2 = R_4$, and $inn = inp = in$:

(54)

$$E_{Trms} = \sqrt{\iint \left[2\ (inR2)^2 + \left(en\left(\frac{R1+R2}{R1}\right)\right)^2 + 8kTR2\left(\frac{R1+R2}{R1}\right) \right] df}$$

$$R1 = R3,\ R2 = R4\ and\ inn = inp = in$$

Evaluating the integral using these simplifications results in:

(55)

$$E_{Trms} = \sqrt{ENB\ 8kTR_2A + 2\left(i_w^2\ R_2^2\right)\left(f_{inc}\ ln\frac{f_H}{f_L} + ENB\right) + e_w^2\ A^2\left(f_{enc}\ ln\frac{f_H}{f_L} + ENB\right)}$$

$$R1 = R3,\ R2 = R4\ and\ inn = inp = in$$

Where $A = (R_1 + R_2)/R_1$, i_w is the white current noise specification (spectral density in $A/\sqrt{Hz}$), f_{inc} is the current noise corner frequency, e_w is the white voltage noise specification (spectral density in $V/\sqrt{Hz}$), and f_{enc} is the voltage noise corner frequency. ENB is determined by the frequency characteristics of the circuit. f_H/f_L is set equal to ENB.

Summary

The techniques presented here can be used to perform a noise analysis on any circuit. Superposition was chosen for illustrative purposes, but the same solutions can be derived by using other circuit analysis techniques.

Noise is a purely random signal; the instantaneous value and/or phase of the waveform cannot be predicted at any time. The only information available for circuit calculations is the average mean-square value of the signal. With multiple noise sources in a circuit, the total root-mean-square (rms) noise signal that results is the square root of the sum of the average mean-square values of the individual sources.

$$E_{Totalrms} = \sqrt{e_{1rms}^2 + e_{2rms}^2 + ...e_{nrms}^2}$$

Because noise adds by the square, when there is an order of magnitude or more difference in value, the lower value can be ignored with very little error. For example:

$$\sqrt{1^2 + 10^2} = 10.05$$

If the 1 is ignored, the error is 0.5%. With modern computational resources, evaluation of all the terms is trivial, but it is important to understand the principles so that time will be spent reducing the 10 before working on the 1.

Noise is normally specified as a spectral density in rms volts or amps per root Hertz, $V\sqrt{Hz}$ or $A\sqrt{Hz}$. To calculate the amplitude of the expected noise signal, the spectral density is integrated over the equivalent noise bandwidth (ENB) of the circuit.

Very often the peak-to-peak value of the noise is of interest. Once the total rms noise signal is calculated, the expected peak-to-peak value can be calculated. The instantaneous value will be equal to or less than 6 times the rms value 99.7% of the time.

References

1. J. B. Johnson. *Thermal Agitation of Electricity in Conductors.* Physical Review, July 1928, Vol. 32.

2. Aldert van der Ziel. *Noise.* Prentice-Hall, Inc., 1954.

3. H. Nyquist. *Thermal Agitation of Electric Charge in Conductors.* Physical Review, July 1928, Vol. 32.

4. Paul R. Gray and Robert G Meyer. *Analysis and Design of Analog Integrated Circuits.* 2d ed., John Wiley & Sons, Inc., 1984.

5. Sergio Franco. *Design with Operational Amplifiers and Analog Integrated Circuits.* McGraw-Hill, Inc., 1988.

6. David E. Johnson, Johnny R. Johnson, and John L. Hilburn. *Electric Circuit Analysis.* Prentice-Hall, Inc., 1989.

References

1. J. B. Johnson. Thermal Agitation of Electricity in Conductors. Physical Review, July 1928, Vol. 32.

2. Aldert van der Ziel. Noise. Prentice-Hall, Inc., 1954.

3. H. Nyquist. Thermal Agitation of Electric Charge in Conductors. Physical Review, July 1928, Vol. 32.

4. Paul R. Gray and Robert G Meyer. Analysis and Design of Analog Integrated Circuits. 2d ed., John Wiley & Sons, Inc., 1984.

5. Sergio Franco. Design with Operational Amplifiers and Analog Integrated Circuits. McGraw-Hill, Inc., 1988.

6. David E. Johnson, Johnny R. Johnson, and John L. Hilburn. Electric Circuit Analysis. Prentice-Hall, Inc., 1989.

Appendix A   Using Current Sources for Resistor Noise Analysis

Figures A1 through A3 show analysis of the resistor noise in the inverting/noninverting op amp noise analysis circuit using current sources in parallel with the noiseless resistors.

$$\overline{E_1} = \overline{I_1}\, R_1 \frac{R_2}{R_1} = \overline{I_1} R_2$$

$$\overline{E_1}^2 = \left(\overline{I_1} R_2\right)^2$$

$$\overline{I_1}^2 = \int \frac{4kT}{R_1}\, df$$

Figure A–1.   E1

$$\overline{E_2} = \overline{I_2}\, R_2$$

$$\overline{E_2}^2 = \left(\overline{I_2} R_2\right)^2$$

$$\overline{I_2}^2 = \int \frac{4kT}{R_2}\, df$$

Figure A–2.   E2

$$\overline{E_3} = \overline{I_3}\, R_3 \left(\frac{R_1 + R_2}{R_1}\right)$$

$$\overline{E_3}^2 = \left[\overline{I_3}\, R_3 \left(\frac{R_1 + R_2}{R_1}\right)\right]^2$$

$$\overline{I_3}^2 = \int \frac{4kT}{R_3}\, df$$
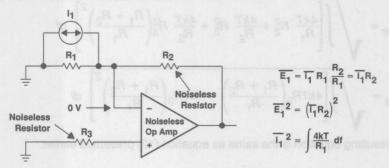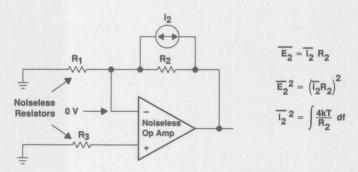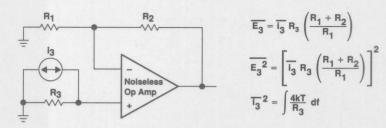
Figure A–3.   E3

Combining the independent noise signals:

$$E_{Rrms} = \sqrt{\overline{E_1}^2 + \overline{E_2}^2 + \overline{E_3}^2}$$

$$E_{Rrms} = \sqrt{\int \left[\frac{4kT}{R_1} R_2^2 + \frac{4kT}{R_2} R_2^2 + \frac{4kT}{R_3} R_3^2 \left(\frac{R_1 + R_2}{R_1} \right)^2 \right] df}$$

$$E_{Rrms} = \sqrt{\int \left[4kTR_2 \left(\frac{R_1 + R_2}{R_1} \right) + 4kTR_3 \left(\frac{R_1 + R_2}{R_1} \right)^2 \right] df}$$

The resulting equation is the same as equation (12) presented earlier.

Choosing an ADC and Op Amp for Minimum Offset
Application Report

Literature Number: SLAA064
June 1999

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Choosing an ADC and Op Amp for Minimum Offset

Heinz-Peter Beckemeyer

ABSTRACT

Designing a mixed-signal circuit containing analog and digital components can be a challenge to the development engineer. Requirements such as a low single-polarity supply voltage and a high degree of precision may conflict, and make the choice of components and the best circuit design difficult. This report discusses problems that arise in using operational amplifiers (op amps) for signal conditioning, and in interfacing a 10-bit A/D converter to a digital signal processor.

Background

Measurement and control applications increasingly use digital systems. However, all the variables that sensors measure (such as temperature, pressure or light intensity) are analog; therefore, an element is needed to link the analog environment to the digital system. This usually means that signals from sensors must be modified for conversion into a digital data format.

An operational amplifier (op amp) generally conditions the signal from a sensor. In the past, op amps used a bipolar supply voltage of ±15 V. The output voltage of such an op amp cannot swing between the maximum voltage levels of the supply; the maximum output voltage limits lie about 2 V above the negative supply voltage, and the same amount below the positive supply voltage. In the same way, the common-mode voltage applied to the input cannot reach the negative or positive supply voltages. In systems using bipolar ±15-V supplies however, this was not a particular restriction, because the remaining dynamic range still provided a wide dynamic range for the signal.

Unipolar Supplies and Op Amps

In most applications nowadays however, a unipolar supply voltage of 5 V, or—particularly with portable systems—a single supply of only 3 V is used.

In applications operating from a unipolar supply voltage, it is particularly important that it be possible to drive the op amp input down to 0 V, the ground (GND) voltage level. This makes it possible to amplify the very low-level signals from sensors.

CMOS op amps are ideally suited for this purpose. With the use of P-channel field-effect transistors in their input stages, the permissible common-mode voltage at the input can be taken down to the negative supply voltage, or to ground (GND) with a unipolar supply voltage. Figure 1 shows the input stage of a CMOS op amp from Texas Instruments.

The differential amplifier consists of P-channel field-effect transistors. Linear driving of the op amp is then only possible when $V_{GS} < V_T$ applies for the input voltage. As the input characteristics show, V_T is the threshold voltage of the field-effect transistor.
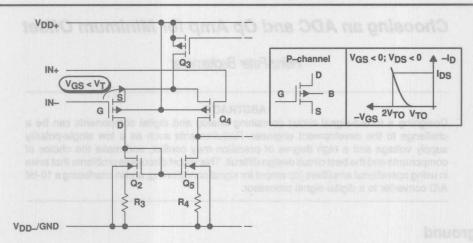
Figure 4. Input Stage of a CMOS Op Amp

With these conditions, it is permissible to drive the op amp down to V_{DD-} or GND. Driving in the positive direction is limited however, and the limit usually lies about 0.8 V to 1.5 V below the positive supply voltage.

This input stage has the advantage of a very high input resistance, making extremely low input currents attainable.

The magnitude of the positive supply voltage—the permissible driving dynamic range—and the sum of the total errors of the op amp limit the usable dynamic signal range of an op amp with a single supply voltage. Reducing the supply voltage from ±15 V to 5 V or 3 V reduces the maximum dynamic range, and thus the performance of the circuit. Figure 2 shows how the dynamic range of a typical linear component deteriorates when the supply voltage is reduced from ±15 V to 5 V, and then to 3 V.

It is important that as much as possible of the reduced supply voltage remains available for the usable dynamic range. Using components that can be driven and controlled up to the limits of the supply voltage can achieve this goal. This ability at the output of the op amp is called rail-to-rail compatibility.

Maximum ±15 V Dynamic Range

Maximum
5 V Dynamic Range

Maximum 3 V Dynamic Range

$V_{IO}, V_n, I_{IB}, I_n, ...$ and amplification errors

15 V

5 V
3 V
0 V

−15 V
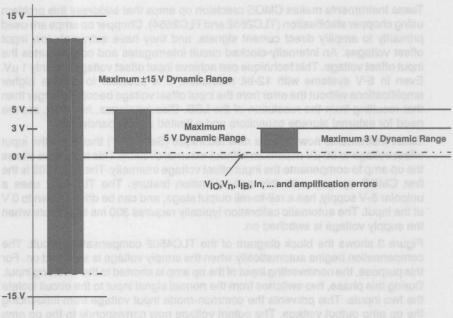
Figure 5. Dynamic Range

Texas Instruments provides a number of rail-to-rail op amps in Advanced-LinCMOS technology, for 5-V and 3-V systems.

Compared to bipolar technology, CMOS op amps have very low supply current. The resulting low power consumption makes them specially suited for battery operated systems.

CMOS Op Amps and Input Offset Voltage

CMOS technology has one disadvantage compared to bipolar components: the relatively high input offset voltage. CMOS op amps have a typical input offset voltage of a few millivolts. The op amp multiplies this input offset voltage, and it becomes an important parameter in determining the precision that can be achieved with the signal conditioning of direct current signals.

Table 1 shows the minimum resolvable potential difference (magnitude of the LSB) of A/D converters. If, for example, 12-bit precision is required in a 3-V system, then a change of the LSB corresponds to a voltage change of 0.73 mV. An op amp having an input offset voltage of 1 mV and an amplification factor of 1 already exceeds the acceptable error resulting from the resolution of the LSB.

Table 1. Resolution of an A/D Converter

BITS	STEPS	RESOLUTION AT $V_{CC} = 5$ V	RESOLUTION AT $V_{CC} = 3$ V	RESOLUTION IN %
10	1024	4.88 mV	2.93 mV	0.098
12	4096	1.22 mV	0.73 mV	0.024

Texas Instruments makes CMOS precision op amps that adddress this problem using chopper stabilisation (TLC2652 and TLC2654). Chopper op amps are used primarily to amplify direct current signals, and they have extremely low input offset voltages. An internally-clocked circuit interrogates and compensates the input offset voltage. This technique can achieve input offset voltages of only 1 µV. Even in 5-V systems with 12-bit resolution, it is possible to choose higher amplifications without the error from the input offset voltage becoming larger than that resulting from the resolution of the LSB. Disadvantages, however, are the need for external storage capacitors and a limited usable bandwidth.

Texas Instruments now offers a new technique (Self-Cal™) that limits the input offset voltage to 50 µV maximum without external circuitry. This technique allows the op amp to compensate the input offset voltage internally. The TLC4502 is the first CMOS op amp with this self-calibration feature. The TLC4502 uses a unipolar 5-V supply, has a rail-to-rail output stage, and can be driven down to 0 V at the input. The automatic calibration typically requires 300 ms to activate when the supply voltage is switched on.

Figure 3 shows the block diagram of the TLC4502 compensating circuit. The compensation begins automatically when the supply voltage is switched on. For this purpose, the noninverting input of the op amp is shorted to the inverting input. During this phase, two switches from the normal signal input to the circuit isolate the two inputs. This prevents the common-mode input voltage from influencing the op amp output voltage. The output voltage now corresponds to the op amp input offset voltage (V_{IO}). An internal analog-to-digital converter (ADC) converts the output voltage to digital, and stores the result in a register. The digital data is applied to the integrated digital-to-analog converter (DAC). The DAC output current makes it possible to compensate an input offset voltage of up to 5 mV. During the calibration phase, an RC oscillator provides the necessary clock signal. The oscillator is deactivated as soon as calibration is complete to reduce noise, and to keep down power consumption.
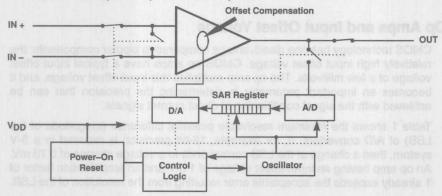
Figure 6. Block Diagram of the TLC4502

Low input offset voltage, reduced temperature drift of the input offset voltage (typically 1 µV/°C), and low input current make the TLC4502 ideal for applications in which small dc voltages must be subjected to high amplification.

Self-Cal is a trademark of Texas Instruments Incorporated.

An Example Unipolar Application

The following application shows the design of a measuring amplifier that uses the TLC4502. This is followed by the solution to the problem of converting the measurement signal from analog into digital in a 10-bit ADC. In this application, a digital signal processor (DSP) controls the ADC.

For amplifying potential differences, such as the diagonal voltage of a Wheatstone bridge, a simple differential amplifier can be used. The differential amplifier is the combination of a noninverting and an inverting amplifier (see Figure 4). Since this circuit has a single supply voltage (5 V), the op amp must have a bias of $V_{CC}/2$ to get the maximum voltage swing at the output. The TLE2425 is ideally suited for this purpose, since it can generate a reference voltage of $V_{REF} = 2.5$ V from a voltage of 4 V to 40 V. The output voltage of the op amp can then be calculated as follows:

$$V_A = \frac{R_3}{R_1 + R_3} \times \left(1 + \frac{R_4}{R_2} \right) \times V_1 - \frac{R_4}{R_2} \times V_2 + V_{REF}$$

The following expression applies for the calculation of the resistors:

$$\frac{R_4}{R_2} = \frac{R_3}{R_1},$$

so that the following particularly convenient result is obtained:

$$V_A = \frac{R_3}{R_1} \times \left(V_1 - V_2 \right) + V_{REF}$$

because with $V_1 = V_2$, the output of the operational amplifier theoretically provides the midpoint voltage $V_A = 2.5$ V.
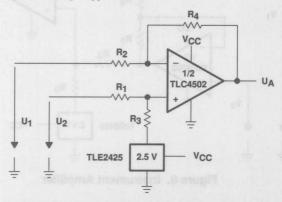
Figure 7. Differential Amplifier

The common-mode rejection of the TLC4502 is typically 100 dB. This means that a common-mode voltage of 1 V has the same effect as a differential voltage of 10 μV between the inputs of the op amp. Changing the ratio of the resistors R4/R2 = R3/R1 has a great influence on the common-mode amplification.

However, the differential amplifier is not suitable for signal sources with high internal resistances. As a result of the finite resistance of the inputs, voltage drops occur in the internal resistance of the source. Very high input resistances can be achieved using two additional op amps. Figure 5 shows this circuit, which is well-known as an instrument amplifier. This circuit uses the previously described differential amplifier, operating with an amplification factor of 1, since all resistors R_3 are the same. Two TLC4502 op amps are connected before the differential amplifier. The signal source (sensor) connected to the instrument amplifier is only loaded with the input resistance of the TLC4502. The typical input resistance of the TLC4502 is 10^{12} Ω.

Appropriate choice of resistor R_2 adjusts the amplification of the instrument amplifier. The output voltage of the instrument amplifier can be calculated as follows:

$$V_A = (V_2 - V_1) \times \left(1 + \frac{2 \times R_1}{R_2}\right) + V_{REF}$$

It is important to use high-precision resistors for R_3 to achieve a high common-mode rejection.
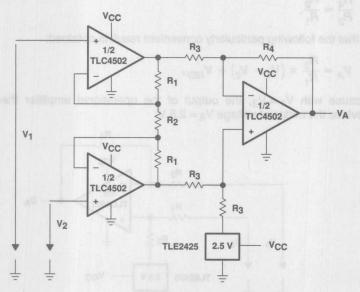
Figure 8. Instrument Amplifier

Analog-to-Digital Conversions

The analog output signal V_A from the differential amplifier or the instrument amplifier must now be converted into a digital signal. To do this, the analog output is connected directly to the analog input of an ADC.

This application uses the TLV1544 (or TLV1548) 10-bit ADC for the conversion. The TLV1544 has four analog inputs; the TLV1548 has eight. Besides the analog input channels, both converters have three self-test channels. The desired channel is activated through the internal multiplexer. These ADCs feature a direct interface to the TMS320 family of DSPs. In addition, they are provided with a direct 3-pole interface to the serial connector of SPI-compatible microprocessors. The TLV1544/8 operates with a supply voltage of from 2.7 V up to 5.5 V, with a low maximum current consumption of only 1 mA. The programmable power-down function reduces the supply current typically to 1 μA. A conversion rate of 85 ksps can be achieved.

In this application the TMS320C542 DSP controls the ADC, and reads out values converted from analog to digital. Figure 6 shows the interface between the ADC and the DSP.

The TMS320C542 serial port (TDM) can be used for control, and for writing in and reading out the conversion values.
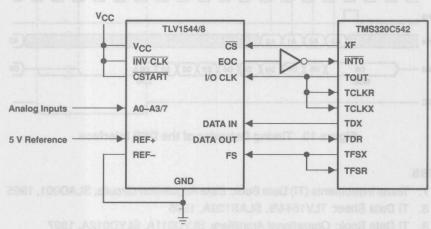
Figure 9. Interface of the TLV1544/8 to the TMS320C542

The DSP XF output signal controls the ADC input chip select ($\overline{CS}$). The DSP TFSX pulse helps initiate the transmission from the DSP. For this to happen, the output must be connected to the TLV1544/8 FS input.

The serial output of the port (TDX) is connected to the data input (DATA IN) of the TLV1544/8. From this output (TDX), the DSP transmits a 4-bit serial data stream to the ADC. These 4 bits contain information for choosing the appropriate analog input, for activating the power-down mode, and for selecting the fast or slow conversion mode.

The serial input of the port (TDR) receives the converted digital values from the data output (DATA OUT). The ADC indicates the end of a conversion cycle with the EOC (end of conversion) output. This signal is inverted and passed to the interrupt input INT0 of the TMS320C542, indicating the end of a conversion cycle. It is now possible to read in the previously converted result, and to continue processing.

The internal timer of the DSP generates the clock signal of the TLV1544/8. For this purpose, the timer output (TOUT) is connected to the clock input (I/O CLK) of the ADC, the maximum clock frequency of which is 8 MHz. The timer output (TOUT) is also connected to the clock inputs of the serial ports (TCLKR and TCLKX).

The inputs REF– and REF+ of the TLV1544/8 determine the upper and lower reference voltages, and thus the maximum input voltage range of the ADC.

Figure 7 shows the timing behaviour at the interface between the ADC and the DSP.
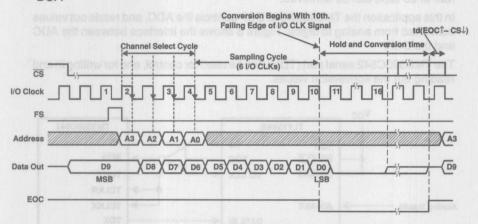
Figure 10. Timing Behavior of the DSP Interface

References

7. Texas Instruments (TI) Data Book: *Data Acquisition Circuits*, SLAD001, 1995
8. TI Data Sheet: TLV1544/8, SLAS139A, 1996
9. TI Data Book: *Operational Amplifiers*, SLYD011A, SLYD012A, 1997
10. TI Data Sheet TLC4502, SLOS161, 1996
11. TI CD–ROM: *Mixed Signal & Analogue Products*, SLYC005A, 1997
    http://www.ti.com/

Electrostatic Discharge (ESD)

Application Report

Literature Number: SSYA008

May 1999

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Electrostatic Discharge (ESD)

Introduction

In recent years, the semiconductor industry has made great strides in developing faster, lower-powered, and smaller devices. During the 1990s, many devices are produced with minimum structure feature size on the silicon chip of 0.25 micron. To put this size in perspective, a typical human hair is about 75 microns in diameter. However, as feature sizes get smaller and smaller, the ESD sensitivity (voltage level at which the device sustains damage) gets lower. Therefore, ESD protection and ESD handling procedures are becoming even more important in preventing ESD damage.

All semiconductor devices have an ESD voltage threshold above which they sustain damage. While circuit designers can provide some on-circuit ESD protection (typically in the 2,000 V to 4,000 V range for the human body model and in the 200 V to 300 V range for the machine model), this is well below the static voltage levels found in work areas without ESD protection. Proper ESD handling and packaging procedures must be used throughout the processing, handling, and storing of unmounted integrated circuits (ICs) and ICs mounted on circuit boards.

What is ESD and How Does It Occur?

A static charge is an unbalanced electrical charge at rest. A static discharge is created when insulator surfaces rub together or pull apart. One surface gains electrons while the other surface loses electrons. This results in an unbalanced electrical condition recognized as static charge.

When a static charge moves from one surface to another, it is called ESD. ESD is a miniature lightning bolt of static charge that moves between two surfaces that have different potentials. ESD only occurs when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When a static charge moves, it becomes a current that damages or destroys oxides, metalizations, and junctions. ESD can occur in one of four different ways: a charged
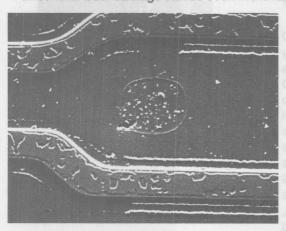
body can touch an IC, a charged IC can touch a grounded surface, a charged machine can touch an IC, or an electrostatic field can induce a voltage across a dielectric that is sufficient to break it down.

Latent Defects

Devices with latent ESD defects are devices that have been degraded by ESD but not destroyed. This occurs when an ESD pulse is not strong enough to destroy a device but causes damage. Often, the device suffers junction degradation through increased leakage or a decreased reverse breakdown, but the device still functions and is still within data-sheet limits. A device can be subjected to numerous weak ESD pulses, with each one further degrading a device before it finally becomes a catastrophic failure. There is no known practical screen for devices with latent ESD defects. To avoid this type of damage, devices must be continually provided with ESD protection as outlined later.

What Voltage Levels of ESD are Possible?

It has been shown that human beings can be charged up to 38,000 volts just by walking across a rug on a low-humidity day. In order for an ESD pulse to be seen, felt, or heard, it must be in the range of 3000–4000 volts. Many devices can be damaged well below this threshold. ESD damage can be seen in the failure analysis photographs shown in Figure 1.
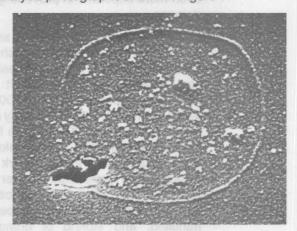
Figure 1. Punctured Barrier Junction After ESD Test at 4000 V
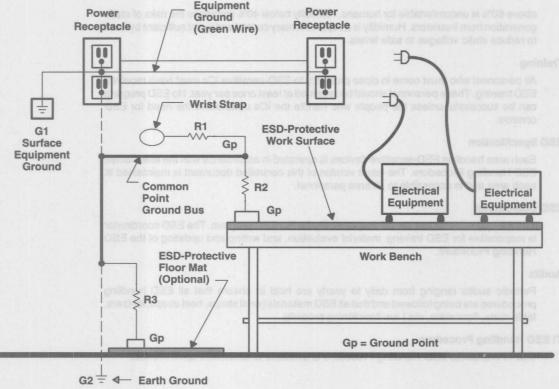
How to Avoid ESD Damage to ICs

The best way to avoid ESD damage is to keep ICs at the same potential as their surroundings. The logical reference potential is ESD ground. The first and most important rule in avoiding ESD damage is to keep ICs and everything that comes in close proximity to them at ESD ground potential. There are four supplementary rules that support this first rule.

- Any person handling the ICs should be grounded either with a wrist strap or ESD-protective footwear used in conjunction with a conductive or static-dissipative floor or floor mat.

- The work surface where devices are placed for handling, processing, testing, etc., must, be made of static-dissipative material and be grounded to ESD ground.

- All insulator materials must either be removed from the work area or must be neutralized with an ionizer. Static-generating clothing must be covered with an ESD-protective smock.

- When ICs are being stored, transferred between operations or workstations, or shipped, they must be kept in a Faraday shield container with inside surfaces (surfaces touching the ICs) that are static-dissipative.

Figure 2 shows an ESD-protected workstation.

NOTES: A. G1 (surface equipment ground) or G2 (earth ground) is acceptable for ESD ground. Where both grounds are used, they are connected (bonded) together.
B. R1 is mandatory for all wrist straps.
C. R2 (for static-dissipative work surfaces) and R3 (for ESD-protective floor mats) are optional. ESD-protective flooring are connected directly to the ESD ground without R3.
D. This ESD-protected workstation complies with JEDEC Standard No. 42.

Figure 2. ESD-Protected Workstation (Side View)

Humidity

Humidity is a very important factor in the generation of static electricity. This is especially true when insulators are present. Humidity affects the surface resistivity of insulator materials. As humidity increases, the surface resistivity decreases. This means that insulator materials rubbed together or pulled apart in a humid environment generate lower static charges than the same materials rubbed together or pulled apart in a dry environment. It is recommended that relative humidity be maintained between 40% and 60%. Humidity

above 60% is uncomfortable for humans. Humidity below 40% increases the risks of static generation from insulators. Humidity is a supplementary control and is not sufficient by itself to reduce static voltages to safe levels.

Training

All personnel who must come in close proximity to ESD-sensitive ICs must have received ESD training. These personnel should be retrained at least once per year. No ESD program can be successful unless the people who handle the ICs understand the need for ESD controls.

ESD Specification

Each area handling ESD-sensitive devices is operated in accordance with the established ESD Handling Procedure. The latest version of this controlled document is maintained in each area and is accessible to all area personnel.

ESD Coordinator

The ESD coordinator has overall responsibility for the ESD program. The ESD coordinator is responsible for ESD training, material evaluation, and writing and updating of the ESD Handling Procedure.

Audits

Periodic audits ranging from daily to yearly are held to ensure that all ESD handling procedures are being followed and that all ESD materials (wrist straps, heel straps, ionizers, table mats, floor mats, etc.) are functioning properly.

TI ESD Handling Procedure

The TI Worldwide ESD Handling Procedure is available to customers upon request.

Understanding Operational Amplifier Specifications

WHITE PAPER: SLOA011

Author: Jim Karki
Mixed Signal and Analog Operational Amplifiers

Digital Signal Processing Solutions
April 1998

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Understanding Operational Amplifier Specifications

Abstract

Selecting the right operational amplifier for a specific application requires you to have your design goals clearly in mind along with a firm understanding of what the published specifications mean. This paper addresses the issue of understanding data sheet specifications.

This paper begins with background information. First, introductory topics on the basic principles of amplifiers are presented, including the ideal op amp model. As an example, two simple amplifier circuits are analyzed using the ideal model. Second, a simplified circuit of an operational amplifier is discussed to show how parameters arise that limit the ideal functioning of the operational amplifier.

The paper then focuses on op amp specifications. Texas Instruments' data book, *Amplifiers, Comparators, and Special Functions*, is the basis for the discussion on op amp specifications. Information is presented about how Texas Instruments defines and tests operational amplifier parameters.

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Introduction

The term operational amplifier, abbreviated op amp, was coined in the 1940s to refer to a special kind of amplifier that, by proper selection of external components, can be configured to perform a variety of mathematical operations. Early op amps were made from vacuum tubes consuming lots of space and energy. Later op amps were made smaller by implementing them with discrete transistors. Today, op amps are monolithic integrated circuits, highly efficient and cost effective.

Amplifier Basics

Before jumping into op amps, lets take a minute to review some amplifier fundamentals. An amplifier has an input port and an output port. In a linear amplifier, output signal = A · input signal, where A is the amplification factor or gain.

Depending on the nature of input and output signals, we can have four types of amplifier gain:

q   Voltage (voltage out/voltage in)

q   Current (current out/current in)

q   Transresistance (voltage out/current in)

q   Transconductance (current out/voltage in)

Since most op amps are voltage amplifiers, we will limit our discussion to voltage amplifiers.
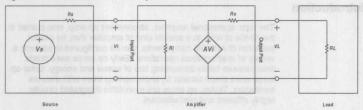
Thevenin's theorem can be used to derive a model of an amplifier, reducing it to the appropriate voltage sources and series resistances. The input port plays a passive role, producing no voltage of its own, and its Thevenin equivalent is a resistive element, R_t. The output port can be modeled by a dependent voltage source, AV_t, with output resistance, R_O. To complete a simple amplifier circuit, we will include an input source and impedance, V_S and R_S, and output load, R_L. Figure 1 shows the Thevenin equivalent of a simple amplifier circuit.

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Understanding Operational Amplifer Specifications

Figure 1. Thevenin Model of Amplifier with Source and Load
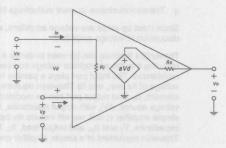
It can be seen that we have voltage divider circuits at both the input port and the output port of the amplifier. This requires us to re-calculate whenever a different source and/or load is used and complicates circuit calculations.

Ideal Op Amp Model

The Thevenin amplifier model shown in Figure 1 is redrawn in Figure 2 showing standard op amp notation. An op amp is a differential to single-ended amplifier. It amplifies the voltage difference, $V_d = V_p - V_n$, on the input port and produces a voltage, V_O, on the output port that is referenced to ground.

Figure 2. Standard Op Amp Notation

We still have the loading effects at the input and output ports as noted above. The ideal op amp model was derived to simplify circuit calculations and is commonly used by engineers in first-order approximation calculations. The ideal model makes three simplifying assumptions:

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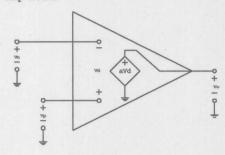
q Gain is infinite $a = \infty$ (1)

q Input resistance is R_i infinite   (2)

q Output resistance is R_o zero   (3)

Applying these assumptions to Figure 2 results in the ideal op amp model shown in Figure 3.

Figure 3. Ideal Op Amp Model

Other simplifications can be derived using the ideal op amp model:

$\Rightarrow I_n = I_p = 0$ (4)

Because $R_i = \infty$, we assume $I_n = I_p = 0$. There is no loading effect at the input.

$\Rightarrow V_o = a\,V_d$ (5)

Because $R_o = 0$ there is no loading effect at the output.

$\Rightarrow V_d = 0$ (6)

If the op amp is in linear operation, V_o must be a finite voltage. By definition $V_o = V_d \times a$. Rearranging, $V_d = V_o / a$. Since $a = \infty$, $V_d = V_o / \infty = 0$. This is the basis of the virtual short concept.
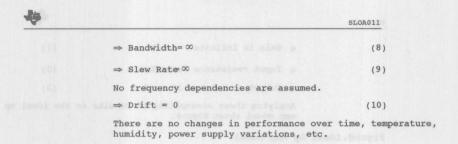
$\Rightarrow$ Common mode gain = 0   (7)

The ideal voltage source driving the output port depends only on the voltage difference across its input port. It rejects any voltage common to V_n and V_p.

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$\Rightarrow$ Bandwidth = ∞ (8)

$\Rightarrow$ Slew Rate = ∞ (9)

No frequency dependencies are assumed.

$\Rightarrow$ Drift = 0   (10)

There are no changes in performance over time, temperature, humidity, power supply variations, etc.

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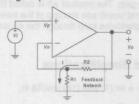
Non-Inverting Amplifier

An ideal op amp by itself is not a very useful device since any finite input signal would result in infinite output. By connecting external components around the ideal op amp, we can construct useful amplifier circuits. Figure 4 shows a basic op amp circuit, the non-inverting amplifier. The triangular gain block symbol is used to represent an ideal op amp. The input terminal marked with a + (V_p) is called the non-inverting input; − (V_n) marks the inverting input.

Figure 4. Non-Inverting Amplifier

To understand this circuit we must derive a relationship between the input voltage, V_i, and the output voltage, V_O.

Remembering that there is no loading at the input,

$$V_p = V_i \qquad (11)$$

The voltage at V_n is derived from V_O via the resistor network, R_1 and R_2, so that,

$$V_n = V_o \ \frac{R_1}{R_1 + R_2} = V_o \ b \qquad (12)$$

where,

$$b = \frac{R_1}{R_1 + R_2} \qquad (13)$$

The parameter b is called the feedback factor because it represents the portion of the output that is fed back to the input.

Recalling the ideal model,

$$V_O = aV_d = a(V_p - V_n) \qquad (14)$$

Substituting,

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$$V_O = a(V_I - bV_O) \tag{15}$$

and collecting terms yield,

$$A = \frac{V_o}{V_I} = \left(\frac{1}{b}\right)\left(\frac{1}{1 + \frac{1}{ab}}\right) \tag{16}$$

This result shows that the op amp circuit of Figure 4 is itself an amplifier with gain A. Since the polarity of V_I and V_O are the same, it is referred to as a non-inverting amplifier.

A is called the *close loop gain* of the op amp circuit, whereas a is the *open loop gain*. The product ab is called the *loop gain*. This is the gain a signal would see starting at the inverting input and traveling in a clockwise loop through the op amp and the feedback network.

Closed Loop Concepts and Simplifications

Substituting $a = \infty$ (1) into (16) results in,

$$A = \frac{1}{b} = 1 + \frac{R_2}{R_1} \tag{17}$$

Recall that in equation (6) we state that V_d, the voltage difference between V_n and V_p, is equal to zero and therefore, $V_n = V_p$. Still they are not shorted together. Rather there is said to be a *virtual short* between V_n and V_p. The concept of the virtual short further simplifies analysis of the non-inverting op amp circuit in Figure 4.

Using the virtual short concept, we can say that,

$$V_n = V_p = V_I \tag{18}$$

Realizing that finding Vn is now the same resistor divider problem solved in (12) and substituting (18) into it, we get,

$$V_I = V_o \frac{R_1}{R_1 + R_2} = V_o b \tag{19}$$

Rearranging and solving for A, we get,

$$A = \left(\frac{1}{b}\right) = 1 + \left(\frac{R2}{R1}\right)$$

The same result is derived in (17). Using the virtual short concept reduced solving the non-inverting amplifier, shown in Figure 4, to solving a resistor divider network.

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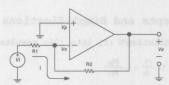
Inverting Amplifier

Figure 5 shows another useful basic op amp circuit, the inverting amplifier. The triangular gain block symbol is again used to represent an ideal op amp. The input terminal, + (Vp), is called the non-inverting input, whereas – (Vn) marks the inverting input. It is similar to the non-inverting circuit shown in Figure 4 except that now the signal is applied to the inverting terminal via R1 and the non-inverting terminal is grounded.

Figure 5. Inverting Amplifier

To understand this circuit, we must derive a relationship between the input voltage, V_i and the output voltage, V_O.

Since V_p is tied to ground,

$$V_p = 0 \tag{20}$$

Remembering that there is no current into the input, the voltage at V_n can be found using superposition. First let $V_O = 0$,

$$V_n = V_i \left(\frac{R_2}{R_1 + R_2} \right) \tag{21}$$

Next let $V_i = 0$,

$$V_n = V_o \left(\frac{R_1}{R_1 + R_2} \right) \tag{22}$$

Combining

$$V_n = V_o \left(\frac{R_1}{R_1 + R_2} \right) + V_i \left(\frac{R_2}{R_1 + R_2} \right) \tag{23}$$

Remembering equation (14), $V_O = \alpha V_d = \alpha(V_p - V_n)$, substituting and rearranging,

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$$A = \frac{V_o}{V_i} = 1 - \left(\frac{1}{b}\right)\left(\frac{1}{1+\frac{1}{ab}}\right) \tag{24}$$

where

$$b = \frac{R_1}{R_1+R_2}$$

Again we have an amplifier circuit. Because the closed loop
gain, A, is negative, and the polarity be opposite to
Therefore, this is an inverting amplifier.

Closed Loop Concepts and Simplifications

Substituting $a=\infty$ (1) into (24) results in

$$A = 1 - \frac{1}{b} = -\frac{R_2}{R_1} \tag{25}$$

Recall that in equation (6) we stated that voltage difference
between V_n and V_p, was equal to zero so that Still they
are not shorted together. Rather there virtual short a
between V_n and V_p. The concept of the virtual short further
simplifies analysis of the inverting op amp circuit in

Using the virtual short concept, we can say that

$$V_n = V_p = 0 \tag{26}$$

In this configuration, the inverting input is a virtual ground

We can write the node equation at the inverting input as

$$\frac{V_n - V_i}{R_1} + \frac{V_n - V_o}{R_2} = 0 \tag{27}$$

Since $V_n = 0$, rearranging, and solving for

$$A = 1 - \frac{1}{b} = -\frac{R_2}{R_1} \tag{28}$$

The same result derived more easily than in (24) Using the
virtual short (or virtual ground) concept reduced solving the
inverting amplifier, Figure into solving a single node
equation.

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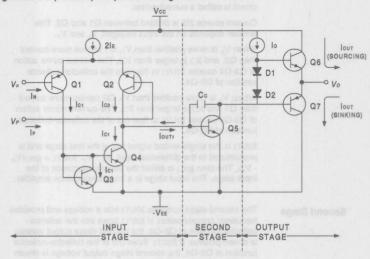
Simplified Op Amp Circuit Diagram

Real op amps are not ideal. They have limitations. To understand and discuss the origins of these limitations, see the simplified op amp circuit diagram shown in Figure 6.

Figure 6. Simplified Op Amp Circuit Diagram

Although simplified, this circuit contains the three basic elements normally found in op amps:

q   Input stage

q   Second stage

q   Output stage

The function of the input stage is to amplify the input difference, $V_p - V_n$, and convert it to a single-ended signal. The second stage further amplifies the signal and provides frequency compensation. The output stage provides output drive capability.

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Input Stage

Symmetry of the input stage is key to its operation. Each transistor pair, Q1-Q2 and Q3-Q4, is matched as closely as possible.

Q3 is diode connected. This forces the collector current in Q3 to equal $IC1$. The base-emitter junctions of Q3 and Q4 are in parallel so they both see the same V_{BE}. Because Q4 is matched to Q3, its collector current is also equal to $IC1$. This circuit is called a current mirror.

Current source $2I_E$ is divided between Q1 and Q2. This division depends on the input voltages, V_p and V_n.

When V_p is more positive than V_n, Q1 carries more current than Q2, and $IC1$ is larger than $IC2$. The current mirror action of Q3-Q4 causes $IOUT1$ to flow into the collector-collector junction of Q2-Q4.

When V_n is more positive than V_P, Q2 carries more current than Q1 and $IC2$ is larger than $IC1$. The current mirror action of Q3-Q4 causes $IOUT1$ to flow out of the collector-collector junction of Q2-Q4.

$IOUT1$ is the single-ended signal out of the first stage and is proportional to the differential input, V_p - V_n. $IOUT1 = gm_1(V_p - V_n)$. The term gm_1 is called the transconductance of the input stage. The input stage is a transconductance amplifier.

Second Stage

The second stage converts $IOUT1$ into a voltage and provides frequency compensation. If $IOUT1$ flows into the collector-collector junction of Q2-Q4, the second stage output voltage is driven positive. If $IOUT1$ flows out of the collector-collector junction of Q2-Q4, the second stage output voltage is driven negative. The second stage is a transresistance amplifier.

The capacitor, C_c, in the second stage provides internal frequency compensation. It causes the gain to role off as the frequency increases. Without C_c, external compensation is required to prevent the op amp from oscillating in most applications.

Output Stage

The output stage is a typical class AB, push-pull amplifier. The emitter follower configuration of Q6 and Q7 provides current drive for the output load, with unity voltage gain. The output stage is a current amplifier.

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Op Amp Specifications

If you have experimented with op amp circuits at moderate gain and frequency, you probably have noted very good agreement between actual performance and ideal performance. As gain and/or frequency are increased, however, certain op amp limitations come into play that effect circuit performance.

In theory, with proper understanding of the internal structures and processes used to fabricate an op amp, we could calculate these effects. Thankfully this is not necessary, as manufacturers provide this information in data sheets. Proper interpretation of data sheet specifications is required when selecting an op amp for an application.

This discussion of op amp parameters is based on Texas Instruments' data sheets. The following definitions (except as noted) are from the "Operational Amplifier Glossary" found in Texas Instruments' data book, *Amplifiers, Comparators, and Special Functions*, pg. 1-37 to pg. 1-40 and pg. 5-37 to pg. 5-40. It defines most of the parameters found in the data sheets.

Operational Amplifier Glossary

a IIO **Average temperature coefficient of input offset current**	The ratio of the change in input offset current to the change in free-air temperature. This is an average value for the specified temperature range. Usually measured in $\mu V/°C$.
a VIO †**Average temperature coefficient of input offset voltage**	The ratio of the change in input offset voltage to the change in free-air temperature. This is an average value for the specified temperature range. Usually measured in $\mu V/°C$.
fm **Phase margin**	The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity.
Am **Gain margin**	The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input.
Av **Large-signal voltage amplification**	The ratio of the peak-to-peak output voltage swing to the change in input voltage required to drive the output.
AVD **Differential voltage amplification**	The ratio of the change in the output to the change in differential input voltage producing it with the common-mode input voltage held constant.

† These definitions were misprinted in the data book noted and were corrected by the author.

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B1 † **Unity gain bandwidth**	The range of frequencies within which the open-loop voltage amplification is greater that unity.
BOM **Maximum-output-swing bandwidth**	The range of frequencies within which the maximum output voltage swing is above a specified value.
Ci **Input capacitance**	The capacitance between the input terminals with either input grounded.
CMRR **Common-mode rejection ratio**	The ratio of differential voltage amplification to common-mode voltage amplification. Note: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.
$\overline{F}$ † **Average noise figure**	The ratio of (1) the total output noise power within a designated output frequency band when the noise temperature of the input termination(s) is at the reference noise temperature at all frequencies to (2) that part of (1) caused by the noise temperature of the designated signal-input termination within a designated signal-input frequency.
ICC+, **I**CC- **Supply current**	The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit.
IIB **Input bias current**	The average of the currents into the two input terminals with the output at the specified level.
IIO **Input offset current**	The difference between the currents into the two input terminals with the output at the specified level.
In **Equivalent input noise current**	The current of an ideal current source (having internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a current source.
IOL **Low-level output current**	The current into an output with input conditions applied that according to the product specification will establish a low level at the output.
IOS **Short-circuit output current**	The maximum output current available from the amplifier with the output shorted to ground, to either supply, or to a specified point.
kSVS † **Supply voltage sensitivity**	The absolute value of the ratio of the change in input offset voltage to the change in supply voltages. Notes: 1. Unless otherwise noted, both supply voltages are varied symmetrically. 2. This is the reciprocal of supply rejection ratio.

† These definitions were misprinted in the data book noted and were corrected by the author.

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ksVR Supply voltage rejection ratio	The absolute value of the ratio of the change in supply voltages to the change in input offset voltage. Notes: 1. Unless otherwise noted, both supply voltages are varied symmetrically. 2. This is the reciprocal of supply sensitivity.
P_D Total power dissipation	The total dc power supplied to the device less any power delivered from the device to a load. Note: At no load: $P_D = V_{CC+} \cdot I$
r_I Input resistance	The resistance between the input terminals with either input grounded.
r_{Id} Differential input resistance	The small-signal resistance between two ungrounded input terminals.
r_o Output resistance	The resistance between an output terminal and ground.
SR Slew rate	The average time rate of change of the closed-loop amplifier output voltage for a step-signal input.
t_r †Rise time	The time required for an output voltage step to change from 10% to 90% of its final value.
t_{tot} Total response time	The time between a step-function change of the input signal and the instant at which the magnitude of the output signal reaches, for the last time, a specified level range (±e) containing the final output signal level.
V_I Input voltage range	The range of voltage that if exceeded at either input may cause the operational amplifier to cease functioning properly.
V_{IO} Input offset voltage	The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.
V_{IC} Common-mode input voltage	The average of the two input voltages.
V_{ICR} Common-mode input voltage range	The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly.
V_n Equivalent input noise voltage	The voltage of an ideal voltage source (having internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can properly be represented by a voltage source.
V_{O1}/V_{O2} Crosstalk Attenuation	The ratio of the change in output voltage of a driven channel to the resulting change in output voltage of another channel.

†These definitions were misprinted in the data book noted and were corrected by the author.

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VOH **High-level output voltage**	The voltage at an output with input conditions applied that according to the product specifications will establish a high level at the output.
VOL **Low-level output voltage**	The voltage at an output with input conditions applied that according to the product specifications will establish a low level at the output.
VID **Differential input voltage**	The voltage at the non-inverting input with respect to the inverting input.
VOM **Maximum peak output voltage swing**	The maximum positive or negative voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.
Vo(PP) **Maximum peak-to-peak output voltage swing**	The maximum peak-to-peak voltage that can be obtained without waveform clipping when quiescent dc output voltage is zero.
ZIc **Common-mode input impedance**	The parallel sum of the small-signal impedance between each input terminal and ground.
Zo **Output impedance**	The small-signal impedance between the output terminal and ground.
Overshoot factor	The ratio of the largest deviation of the output signal value from its final steady-state value after a step-function change of the input signal to the absolute value of the difference between the steady-state output signal values before and after the step-function change of the input signal.
THD + N **‡Total harmonic distortion plus noise**	The ratio of the RMS noise voltage and RMS harmonic voltage of the fundamental signal to the total RMS voltage at the output.
GBW **‡ Gain bandwidth product**	The product of the open-loop voltage amplification and the frequency at which it is measured.
‡ Average long-term drift coefficient of input offset voltage	The ratio of the change in input offset voltage to the change time. This is an average value for the specified time period. Usually measured in μV/month.

Texas Instruments usually specifies parameters under specific test conditions with some combination of minimum, typical and maximum values at 25 C, and over the full temperature range. What does this mean?

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‡ These definitions where added by the author. They appear commonly in the data sheets.

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This means that a parameter measurement circuit is constructed, and the parameter is measured in a large number of devices at various temperatures over the temperature range of the device. Most parameters have a statistically normal distribution. The typical value published in the data sheet is the mean or average value of the distribution, with one exception, offset voltage. The average offset voltage is normally zero (or very close to zero). Therefore, the typical value listed for offset voltage is the 1s value. This means that in 68% of the devices tested the parameter was found to be – the typical value or better. The definition of minimum and maximum values has changed over the years. Texas Instruments currently publishes a conservative 6s value.

Certain devices are screened for parameters such as offset voltage. These devices are normally given an A suffix. This ensures that the device meets the maximum value specified in the data sheet.

The following discussion uses Figure 6 extensively to explain the origins of the various parameters.

Absolute Maximum Ratings and Recommended Operating Conditions

The following typical parameters are listed in the absolute maximum ratings and the recommended operating conditions for TI op amps. The op amp will perform more closely to the typical values for parameters if operated under the recommended conditions. Stresses beyond the maximums listed will cause unpredictable behavior and may cause permanent damage.

q Absolute Maximums

   n Supply Voltage

   n Differential input voltage

   n Input voltage range

   n Input current

   n Output current

   n Total current into V_{DD+}

   n Total current out of V_{DD-}

   n Duration of short-circuit current (at or below 25°C)

   n Continuous total power dissipation

   n Operating free-air temperature

   n Storage temperature

   n Lead temperature

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q Recommended Operating Conditions

n Supply Voltage

n Input voltage range

n Common-mode input voltage

n Operating free-air temperature

Input Offset Voltage

Input offset voltage, V_{IO}, is defined as "the DC voltage that must be applied between the input terminals to force the quiescent DC output voltage to zero or some other level, if specified". If the input stage was perfectly symmetrical and the transistors were perfectly matched, $V_{IO} = 0$. Because of process variations, geometry and doping are never exact to the last detail. All op amps require a small voltage between their inverting and non-inverting inputs to balance the mismatches. V_{IO} is normally depicted as a voltage source driving the non-inverting input, as shown in Figure 7.

TI data sheets show two other parameters related to V_{IO}; the average temperature coefficient of the input offset voltage and the input offset voltage long-term drift.

The average temperature coefficient of input offset voltage, aV_{IO}, specifies the expected input offset drift over temperature. Its units are mV/ C. V_{IO} is measured at the temperature extremes of the part, and aV_{IO} is computed as $DV_{IO}/D C$.
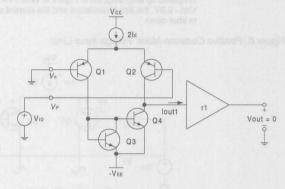
Normal aging in semiconductors causes changes in the characteristics of devices. The input offset voltage long-term drift specifies how V_{IO} is expected to change with time. Its units are $mV/month$.

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Figure 7. VIO

Input offset voltage is of concern anytime DC precision is required. Several methods are used to null its effects.

Input Current

Referring to Figure 6, we can see that a certain amount of bias current is required at each input. The input bias current, I_{IB}, is computed as the average of the two inputs,

$$I_{IB} = (I_N+I_P)/2$$

Input offset current, I_{IO}, is defined as the difference between the bias currents at the inverting and non-inverting inputs,

$$I_{IO} = I_N-I_P$$

Bias current is of concern when the input source impedance is high. Usually offset currents are an order of magnitude less than bias current so matching the input impedance of the inputs helps to nullify the effect of input bias current on the output voltage.

Input Common Mode Voltage Range

Normally there is a voltage that is common to the inputs of the op amp. If this common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range, V_{ICR}, specifies the range over which normal operation is guaranteed.

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Figure 8 illustrates the positive input voltage limit using the simplified op amp diagram of Figure 6. When V$_{IN}$ is higher than V$_{CC}$ - 0.9V, the input transistors and the current source will begin to shut down.

Figure 8. Positive Common-Mode Voltage Input Limit

$$V_{IN+} < V_{CC} - 0.3V - 0.6V$$
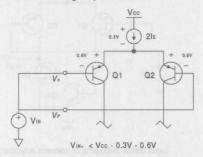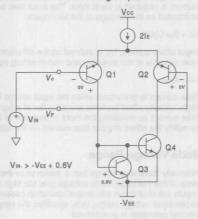
Figure 9 illustrates the negative input voltage limit using the simplified op amp diagram of Figure 6. When VIN is less than -VEE + 0.6V, the current mirror (Q3-Q4) will begin to shut down.

Figure 9. Negative Common-Mode Voltage Input Limit

$$V_{IN-} > -V_{EE} + 0.6V$$

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Structures like the one shown in the example above do not allow the common-mode input voltage to include either power supply rail. Other technologies used to construct op amp inputs offer different common-mode input voltage ranges that do include one or both power supply rails. Some examples are as follows (reference schematics can be found in the Texas Instruments' data book Amplifiers, Comparators, and Special Functions):
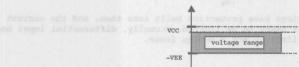
q The LM324 and LM358 use bipolar PNP inputs that have their collectors connected to the negative power rail. Since V equal zero, this allows the common-mode input voltage range to include the negative power rail.

q The TL07X and TLE207X type BiFET op amps use p-channel JFET inputs with the sources tied to the positive power rail a bipolar current sources. Since equal zero, this structure typically allows the common-mode input voltage range to include the positive power rail.

q TI LinCMOS op amps use p-channel CMOS inputs with the substrate tied to the positive power rail. Therefore a conducting channel is created for V and this allows the common-mode input voltage range to include the negative power rail.

q Rail-to-rail input op amps use complementary N and P type devices in the differential inputs. When the common-mode input voltage nears either rail at least one of the different inputs is still active.

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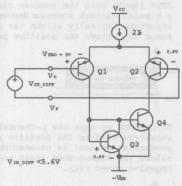
Differential Input Voltage Range

Differential input voltage range is normally specified in data as an absolute maximum. Figure 40 illustrates this.

If the differential input voltage is greater than the base-emi reverse break down voltage of input transistor Q1 plus the bas emitter forward breakdown voltage of Q2, then Q1's BE junction will act like a zener diode. This is a destructive mode of ope: and results in deterioration of Q1's current gain. The same is if V_{IN_DIFF} is reversed, except Q2 breaks down.

Figure 40. Differential-Mode Voltage Limit

Some devices have protection built into them, and the current the input needs to be limited. Normally, differential input mo voltage limit is not a design issue.

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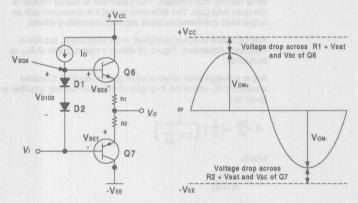
Maximum Output Voltage Swing

The maximum output voltage, V_{OM-}, is defined as "the maximum positive or negative peak output voltage that can be obtained without wave form clipping when quiescent DC output voltage is zero". V_{OM-} is limited by the output impedance of the amplifier, the saturation voltage of the output transistors, and the power supply voltages. This is shown in Figure 11. Note that V_{OM-} depends on the output load.

Figure 11. V_{OM-}

The maximum value that V_{BQ6} can be is $+V_{CC}$, therefore $V_O <= +V_{CC} - V_{R1} - V_{BEQ6} - V_{SATQ6}$. The minimum value that V_i can be is $-V_{EE}$, therefore $V_O >= -V_{EE} + V_{R2} + V_{BEQ7} + V_{SATQ7}$.

This emitter follower structure cannot drive the output voltage to either rail. Rail to rail output op amps use a common emitter (bipolar) or common source (CMOS) output stage. With these structures, the output voltage swing is only limited by the saturation voltage (bipolar) or the on resistance (CMOS) of the output transistors, and the load being driven.

Because newer products are focused on single supply operation, more recent data sheets from Texas Instruments use the terminology V_{OH} and V_{OL} to specify the maximum and minimum output voltage.

Maximum and minimum output voltage is usually a design issue when dynamic range is lost if the op amp cannot drive to the rails. This is the case in single supply systems where the op amp is used to drive the input of an analog-to-digital converter, which is configured for full scale input voltage between ground and the positive rail.

Large Signal Differential Voltage Amplification

Large signal differential voltage amplification, A_{VD}, is the ratio of the output voltage change to the input differential voltage change, while holding V_{CM} constant. This parameter is closely related to the open loop gain. The difference is that it is measured with an output load and therefore takes into account loading effects.

The DC value of A_{VD} is published in the data sheet, but A_{VD} is frequency dependent. Figure 18 shows a typical graph of A_{VD} vs. frequency.

A_{VD} is a design issue when precise gain is required. Consider equation (16), where the loop gain of the non-inverting amplifier is given by:

$$A = \frac{V_o}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1 + \frac{1}{ab}}\right)$$

where,

$$b = \frac{R_1}{R_1 + R_2}$$

It is desired to control the gain of the circuit by selecting the appropriate resistors. The term $1/ab$ in the equation is seen as an error term. Unless a, or A_{VD}, is large in comparison with $1/b$, it will have an undesired effect on the gain of the circuit.

Input Parasitic Elements

Both inputs have parasitic impedance associated with them. Figure 12 shows a model where it is lumped into resistance and capacitance between each input terminal and ground and between the two terminals. There is also parasitic inductance, but the effects are negligible at low frequency.

Input impedance is a design issue when the source impedance is high. The input loads the source.

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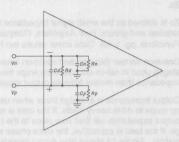
Also input capacitance will cause extra phase shift in the feedback path. This erodes phase margin and can be a problem when using high value feedback resistors.

Figure 12. Input Parasitic Elements

Input Capacitance

Input capacitance, Ci, is measured between the input terminals with either input grounded. Ci is usually on the order of a few pF. To relate Ci to Figure 12, if you ground Vp, Ci = Cd || Cn.

Sometimes common-mode input capacitance, Cic, is specified. To relate Cic to Figure 12, if you short Vp to Vn, Cic = Cp || Cn, the input capacitance a common mode source would see to ground.

Input Resistance

Two parameters for input resistance, ri and rid, are defined in Texas Instruments' data book, *Amplifiers, Comparators, and Special Functions*, pg. 1-39. Input resistance, ri, is "the resistance between the input terminals and either input grounded." Differential input resistance, rid, is "the small-signal resistance between two ungrounded input terminals."

To relate ri to Figure 12, if you ground Vp, ri = Rd || Rn. Depending on the type of input, values usually run on the order of $10^7 w$ to $10^{12} w$.

To relate rid to Figure 12, with both input terminals floating, rid = Rd || (Rn + Rp). Depending on the type of input, values usually run on the order of $10^7 w$ to $10^{12} w$.

Sometimes common-mode input resistance, ric, is specified. To relate ric to Figure 12, if you short Vp to Vn, ric = Rp || Rn, the input resistance a common mode source would see to ground.

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Output Impedance

Different data sheets list the output impedance under two different conditions. Some data sheets list *closed-loop* output impedance while others list *open loop* output impedance, both designated by Zo.

Zo is defined as the small signal impedance between the output terminal and ground (see *Amplifiers, Comparators, and Special Functions*, pg. 1-40). Data sheet values run from 50w to 200w.

Common emitter (bipolar) and common source (CMOS) output stages used in rail-to-rail output op amps have higher output impedance than emitter follower output stages.

Output impedance is a design issue when using rail-to-rail output op amps to drive heavy loads. If the load is mainly resistive, the output impedance will limit how close to the rails the output can go. If the load is capacitive, the extra phase shift will erode phase margin. Figure 13 shows how output impedance affects the output signal assuming Zo is mostly resistive.

Figure 13. Effect of Output Impedance

$$Vo = aVd \frac{RL}{(RL+Zo)}$$

Resistive Load

$$Vo = aVd \frac{1}{(jf/fo)+1}$$

Where

$$fo = \frac{1}{2pi \, ZoCL}$$

Capacitive Load

Common-Mode Rejection Ratio

Common-mode rejection ratio, CMRR, is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification, A_{DIF}/A_{COM}. Ideally this ratio would be infinite with common mode voltages being totally rejected.

The common-mode input voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage. The real mechanism at work is $DVos/DVCOM$.

In a Texas Instrument data sheet, CMRR = $DVCOM/DVos$ (gives a positive number in dB).

CMRR, as published in the data sheet, is a DC parameter. CMRR, when graphed vs. frequency, falls off as the frequency increases.

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A common source of common-mode interference voltage is 50 Hz or 60 Hz noise from the AC mains. Care must be used to ensure that the CMRR of the op amp is not degraded by other circuit components.

Supply Voltage Rejection Ratio

Supply voltage rejection ratio, k_{SVR} (AKA power supply rejection ratio, PSRR), is the ratio of power supply voltage change to output voltage change.

The power voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage. The real mechanism at work is DV_{OS}/DV_{CC-}.

In a Texas Instrument data sheet, for a dual supply op amp, $k_{SVR} = DV_{CC-}/DV_{OS}$ (to get a positive number in dB). The term DV_{CC-} means that the plus and minus power supplies are changed symmetrically. For a single supply op amp, $k_{SVR} = DV_{DD}/DV_{OS}$ (to get a positive number in dB).

Also note that the mechanism that produces k_{SVR} is the same as for CMRR. Therefore, k_{SVR}, as published in the data sheet, is a DC parameter like CMRR; when k_{SVR} is graphed vs. frequency, it falls off as the frequency increases.

Switching power supplies can have noise on the order of 20 kHz to 200 kHz and higher. K_{SVR} is almost zero at these high frequencies, so that noise on the power supply results in noise on the output of the op amp.

Supply Current

Supply current, I_{DD}, is the quiescent current draw of the op amp(s) with no load. In a Texas Instrument data sheet, this parameter is usually the total quiescent current draw for the whole package. There are exceptions, as with the TL05X, TL06X, and TL07X, where I_{DD} is the quiescent current draw for each amplifier.

In op amps you trade power consumption for noise and speed.

Slew Rate at Unity Gain

Slew rate, SR, is the rate of change in the output voltage caused by a step input. Its units are V/μs or V/ms. Figure 14 shows slew rate graphically.

Referring back to Figure 6, voltage change in the second stage is limited by the charging and discharging of capacitor Cc. The maximum rate of change occurs when either side of the differential pair is conducting 2I_E. This is the major limit to slew rate. Essentially, $SR = 2I_E/C_C$. However, there are op amps that work on different principles where this is not true.

The requirement to have current flowing in or out of the input stage to change the voltage out of the second stage requires an error voltage at the input anytime the output voltage of an op amp is changing. An error voltage on the order of 120 mV is required for an op amp with a bipolar input to realize full slew rate. This can be as high as 1V to 3V for a JFET or MOSFET input.

Capacitor, Cc, is added to make the op amp unity gain stable. Some op amps come in de-compensated versions where the value of Cc is reduced . This increases realizable bandwidth and slew rate, but the engineer must ensure the stability of the circuit by other means.

In op amps you trade power consumption for noise and speed. To increase slew rate, the bias currents within the op amp are increased.

Figure 14. Slew Rate

$$SR = dV/dt$$

Equivalent Input Noise

All op amps have associated parasitic noise sources. Noise is measured at the output of an op amp and referenced back to the input; thus, it is called equivalent input noise.

Equivalent input noise specifications are usually given in two ways. One way is to specify the spot noise; that is, the equivalent input noise is given as voltage, V_n, (or current, I_n) per root hertz at a specific frequency. The second way is to specify noise as a peak-to-peak value over a frequency band. A brief review of noise characteristics is necessary to explain these parameters.

Understanding Operational Amplifier Specifications

The spectral density of noise in op amps has a 1/f and a white noise component. 1/f noise is inversely proportional to frequency and is usually only significant at low frequencies. White noise is spectrally flat. Figure 15 shows a typical graph of op amp equivalent input noise.
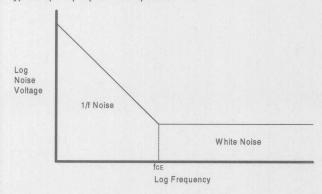
Usually spot noise is specified at two frequencies. The first frequency is usually 10 Hz, where the noise exhibits 1/f spectral density. The second frequency is typically 1 kHz, where the noise is spectrally flat. The units used are normally RMS nV/ Hz (or RMS pA/ Hz for current noise). In Figure 15 the transition between 1/f and white is denoted as the corner frequency, f_{CE}.

A noise specification, such as $V_{N(PP)}$, is the a peak to peak voltage over a specific frequency band, typically 0.1 Hz to 1 Hz or 0.1 Hz to 10 Hz. The units of measurement are typically nV pk-pk. To convert noise voltages given in RMS to pk-pk, a factor around 6 is typically used to account for the high crest factor seen in noise voltages e.g. $V_{N(PP)} = 6 \times V_{N(RMS)}$.

Given the same structure within an op amp, increasing bias currents lowers noise (and increases SR, GBW, and power dissipation).

Also the resistance seen at the input to an op amp adds noise. Balancing the input resistance on the non-inverting input to that seen at the inverting input, while helping with offsets due to input bias current, adds noise to the circuit.

Figure 15. Typical Op Amp Input Noise Spectrum

Total Harmonic Distortion plus Noise

Total harmonic distortion plus noise, THD + N, compares the frequency content of the output signal to the frequency content of the input. Ideally, if the input signal is a pure sine wave, the output signal is a pure sine wave. Because of non-linearity and noise sources within the op amp, the output is never pure.

THD + N is the ratio of all other frequency components to the fundamental and is usually specified as a percentage:

$$THD + N = \frac{(\text{Harmonic voltages} + \text{Noise voltages})}{\text{Total output voltage}} \cdot 100\%$$

Figure 16 shows a hypothetical graph where THD + N = 1%. The fundamental is the same frequency as the input signal and makes up 99% of the output signal. Non-linear behavior of the op amp results in harmonics of the fundamental being produced in the output. The noise in the output is mainly due to the input referenced noise of the op amp. All the harmonics and noise added together make up 1% of the output signal.
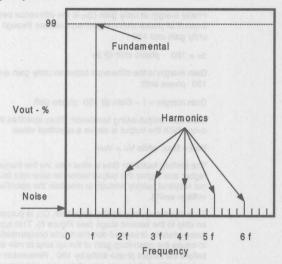
Two major reasons for distortion in an op amp are the limit on output voltage swing and slew rate. Typically an op amp must be operated at or below its recommended operating conditions to realize low THD.

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SLOA011

Figure 16. Output Spectrum with THD + N = 1%

Unity-Gain Bandwidth and Phase Margin

There are five parameters that relate to the frequency characteristics of the op amp that you will encounter in Texas Instruments' data sheets:

q Unity-gain bandwidth (B_1)

q Gain bandwidth product (GBW)

q Phase margin at unity gain (f_m)

q Gain margin

q Maximum output-swing bandwidth (B_{OM})

Unity-gain bandwidth (B_1) and gain bandwidth product (GBW) are similar. B_1 specifies the frequency at which A_{VD} of the op amp is 1:

$$B_1 = f @ A_{VD} = 1$$

GBW specifies the gain-bandwidth product of the op amp in an open loop configuration and the output loaded:

$$GBW = A_{VD} \cdot f$$

Phase margin at unity gain (f_m) is the difference between the amount of phase shift a signal experiences through the op amp at unity gain and 180 :

$$f_m = 180 \text{ - phase shift @ } B_1$$

Gain margin is the difference between unity gain and the gain at 180 phase shift:

$$\text{Gain margin} = 1 - \text{Gain @ } 180 \text{ phase shift}$$

Maximum output-swing bandwidth (B_{OM}) specifies the bandwidth over which the output is above a specified value:

$$B_{OM} = f_{MAX}, \text{ while } V_O > V_{MIN}$$

The limiting factor for B_{OM} is slew rate. As the frequency gets higher and higher the output becomes slew rate limited and can not respond quickly enough to maintain the specified output voltage swing.

To make the op amp stable, capacitor, C_C, is purposely fabricated on chip in the second stage (see Figure 6). This type of frequency compensation is termed dominant pole compensation. The idea is to cause the open-loop gain of the op amp to role off to unity before the output phase shifts by 180 . Remember that Figure 6 is very simplified: there are other frequency shaping elements within a real op amp. Figure 17 shows a typical gain vs. frequency plot for an internally compensated op amp as normally presented in a Texas Instruments data sheet. Figure 18 contains the same information except the phase axis is shifted for clarity.

As noted earlier, it can be seen that A_{VD} falls off with frequency. A_{VD} (and thus B1 or GBW) is a design issue when precise gain is required of a specific frequency band. Consider equation (16), where the loop gain of the non-inverting amplifier is given by:
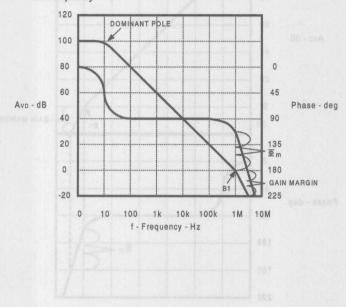
$$A = \frac{V_o}{V_i} = \left(\frac{1}{b}\right)\left(\frac{1}{1 + \frac{1}{ab}}\right)$$

It is desired to control the gain of the circuit by selecting the appropriate resistors. The term $1/ab$ in the equation is seen as an error term. Unless a, or A_{VD}, is large for all frequencies of interest in comparison with $1/b$, a will have an effect on the gain of the circuit, which is undesired.

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Phase margin (f_m) and gain margin are different ways of specifying the stability of the circuit. Since rail-to-rail output op amps have higher output impedance, a significant phase shift is seen when driving capacitive loads. This extra phase shift erodes the phase margin, and for this reason most CMOS op amps with rail-to-rail outputs have limited ability to drive capacitive loads.

Figure 17. Typical Large-Signal Differential Voltage Amplification and Phase Shift vs. Frequency
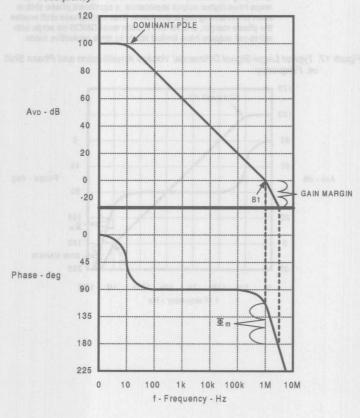
Figure 18. Easier to Read Graph of Voltage Amplification and Phase Shift vs. Frequency

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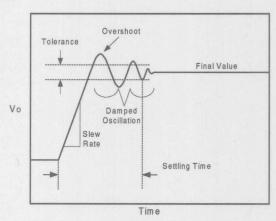
Settling Time

It takes a finite time for a signal to propagate through the internal circuitry of an op amp. Therefore, it takes a certain period of time for the output to react to a step change in the input. Also the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Settling time, ts, is the time required for the output voltage to settle to within a specified percentage of the final value given a step input. Figure 19 shows this graphically.

Figure 19. Settling Time

Settling time is a design issue in data acquisition circuits when signals are changing rapidly. An example is when using an op amp following a multiplexer to buffer the input to an analog to digital converter. Step changes can occur at the input to the op amp when the multiplexer changes channels. The output of the op amp must settle to within a certain tolerance before the analog to digital converter samples the signal.

References

Paul R. Gray and Robert G Meyer. *Analysis and Design of Analog Integrated Circuits*. 2d ed., John Wiley & Sons, Inc., 1984.

Sergio Franco. *Design with Operational Amplifiers and Analog Integrated Circuits*. McGraw-Hill, Inc., 1988.

Texas Instruments, Inc. *Amplifiers, Comparators, and Special Functions Data Book*. Volume A and B, 1997.

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PowerPAD Thermally Enhanced Package

TECHNICAL BRIEF: SLMA002

Mixed Signal Products

Semiconductor Group
21 November 1997

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PowerPAD™ Thermally Enhanced Package

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PowerPAD Thermally Enhanced Package

Abstract

The PowerPAD thermally enhanced package provides greater design flexibility and increased thermal efficiency in a standard size IC package. PowerPAD's improved performance permits higher clock speeds, more compact systems and more aggressive design criteria.

PowerPAD packages are available in several standard surface mount configurations. They can be mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. This document will focus on the specifics of integrating a PowerPAD package into the PCB design.

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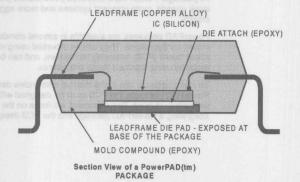
1. Introduction

The PowerPAD concept is implemented in a standard epoxy-resin package material. The integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This provides an extremely low thermal resistance (Θ_{jc}) path between the IC junction and the exterior of the case. Because the external surface of the leadframe die pad is on the PCB side of the package, it can be attached to the board using standard flow soldering techniques. This allows efficient attachment to the board, and permits board structures to be used as heat sinks for the IC. Using vias, the leadframe die pad can be attached to a ground plane or special heat sink structure designed into the PCB. For the first time, the PCB designer can implement power packaging without the constraints of extra hardware, special assembly instructions, thermal grease or additional heat sinks.

Figure 1. Schematic Representation of the PowerPAD Package Components

LEADFRAME (COPPER ALLOY)
IC (SILICON)
DIE ATTACH (EPOXY)

LEADFRAME DIE PAD - EXPOSED AT
BASE OF THE PACKAGE
MOLD COMPOUND (EPOXY)

Section View of a PowerPAD(tm)
PACKAGE

Because the exact thermal performance of any PCB is dependent on the details of the circuit design and component installation, exact performance figures cannot be given here. However, representative performance is very important in making design decisions. The data shown in Table 1 is typical of the performance that can be expected from the PowerPAD package.

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Table 1. Typical Power Handling Capabilities of PowerPAD Packages

Package Type	Pin Count	Standard Package	PowerPAD Package
SSOP	20	0.75 W	3.25 W
TSSOP	24	0.55 W	2.32 W

Notes: 1) Assumes 150° C junction temperature and 80° C ambient temperature.
2) Values are calculated from $\Theta_{jа}$ figures shown in Appendix A.

For example, the user can expect 3.25 watts of power handling capability for the PowerPAD version of the 20-pin SSOP package. The standard version of this package can only handle 0.75 watts. Details for all package styles and sizes are given in Appendix A.

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2. Installation and Use

2.1 PCB Attachment

Proper thermal management of the PowerPAD package requires PCB preparation. This preparation is not difficult, nor does it use any extraordinary PCB design techniques, however it is necessary for proper heat removal.

Figure 2. Bottom and Top View of the 20 pin TSSOP PowerPAD Package

20 PIN TSSOP, PowerPAD(tm) PACKAGE

RELEASED FOR VOLUME PRODUCTION SEPTEMBER, 1995.

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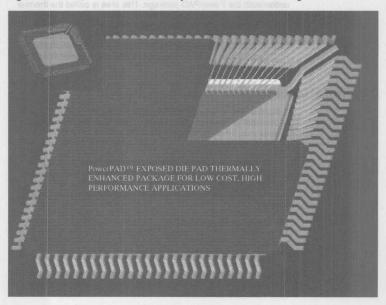
Figure 3. 64 Pin, 14 x 14 x 1.0mm Body TQFP PowerPAD Package

PowerPAD™ EXPOSED DIE PAD THERMALLY
ENHANCED PACKAGE FOR LOW COST, HIGH
PERFORMANCE APPLICATIONS

All of the thermally enhanced packages incorporate features that provide a very low thermal resistance path for heat removal from the integrated circuit - either to and through a printed circuit board (in the case of zero airflow environments), or to an external heatsink. The TI PowerPAD implementation does this by creating a leadframe where the bottom of the die pad is even with a surface of the package (as opposed to the case where a heat slug is embedded in the package body to create the thermal path). (See Figure 2 and Figure 3.)

2.2 PCB Design Considerations

The printed circuit board that will be used with PowerPAD packages must have features included in the design to remove the heat from the package efficiently.

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As a minimum, there must be an area of solder-tinned-copper underneath the PowerPAD package. This area is called the thermal land. As detailed below, the thermal land will vary in size depending on the PowerPAD package being used, the PCB construction and the amount of heat that needs to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed below.
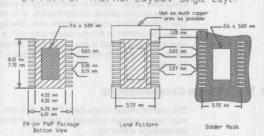
2.3 Thermal Lands

A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD package. During normal surface mount flow solder operations the leadframe on the underside of the package will be soldered to this thermal land creating a very efficient thermal path. Normally, the PCB thermal land will have a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. The size of the thermal land should be as large as needed to dissipate the required heat.

For simple, double-sided PCBs, where there are no internal layers, the surface layers must be used to remove heat. Shown in Figure 4 is an example of a thermal land for a 24-pin package. Details of the package, the thermal land and the required solder mask are shown. If the PCB copper area is not sufficient to remove the heat, the designer can also consider external means of heat conduction, such as attaching the copper planes to a convenient chassis member or other hardware connection.

Figure 4. Package and PCB Land Configuration for a Single Layer PCB

24-Pin PWP Thermal Layout Single Layer

Use as much copper area as possible

2.6 x 5.09 mm

1.20 mm

2.6 x 5.09 mm

8.10 mm
7.70 mm

0.65 mm

0.65 mm

0.30 mm
0.19 mm

0.27 mm

4.50 mm
4.30 mm

6.70 mm
6.10 mm

5.72 mm

5.72 mm

24-pin PWP Package
Bottom View

Land Pattern

Solder Mask

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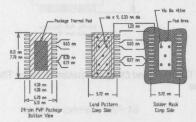
For multilayer PCBs, the designer can take advantage of internal copper layers (such as the ground plane) for heat removal. The external thermal land on the surface layer is still required, however the thermal vias can conduct heat out through the internal power or ground plane. Shown in Figure 5 is an example of a thermal land used for multilayer PCB construction. In this case, the primary method of heat removal is down through the thermal vias to an internal copper plane.

Figure 5. Package and PCB Land Configuration for a Multi-Layer PCB

24-Pin PWP Thermal Layout Multi-Layer

Shown in Figure 6 are the details of a 64 pin TQFP PowerPAD package. The recommended PCB thermal land for this package is shown in Figure 7.

The maximum land size for TQFP packages is the package body size minus 2.0 mm. This land is normally attached to the PCB for heat removal, but can be configured to take the heat to an external heat sink. This is preferred when airflow is available.

PowerPAD Thermally Enhanced Package   13
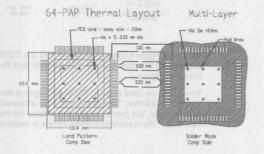
Figure 6. 64 pin TQFP Package with PowerPAD Implemented, Bottom View

64-PAP PowerPAD(tm) PACKAGE

64-Pin PAP Package
Bottom View

Figure 7. PCB Thermal Land Design Considerations for Thermally Enhanced
TQFP Packages

64-PAP Thermal Layout   Multi-Layer

Land Pattern
Comp Side

Solder Mask
Comp Side

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2.4 Thermal Vias

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sources. The number of vias used, the size of the vias and the construction of the vias are all important factors in both the PowerPAD package thermal performance and the package-to-PCB assembly. Recommendations and guidelines for thermal vias follow.

Shown in Figure 8 and Figure 9 are the effects on PCB thermal resistance of varying the number of thermal vias for various sizes of die for 2- and 4-layer PCBs. As can be seen from the curves, there is a point of diminishing returns where additional vias will not significantly improve the thermal transfer through the board. For a small die, having from five to nine vias should prove adequate for most applications. For larger die, a higher number may be used simply because there is more space available under the larger package. Shown in Figure 10 are examples of ideal thermal land size and thermal via patterns for PowerPAD™ packages using 0.33mm (13 mil) diameter vias plated with 1 oz. copper. This thermal via pattern set represents a copper cross section in the barrel of the thermal via of approximately 1% of the total thermal land area. Fewer vias may be utilized and still attain a reasonable thermal transfer into and through the PCB as shown in Figures 8 and 9.

The number of thermal vias will vary with each product being assembled to the PCB, depending on the amount of heat that must be moved away from the package, and the efficiency of the system heat removal method. Characterization of the heat removal efficiency versus the thermal via copper surface area should be performed to arrive at an optimum value for a given board construction. Then the number of vias required can be determined for any new design to achieve the desired thermal removal value.

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Figure 8. Impact of the Number of Thermal Vias versus Chip Area (Die Area)

JEDEC 2-LAYER BOARD THERMAL RESISTANCE (JC)
COMPARISON

Note: Apply bare die to the JEDEC board
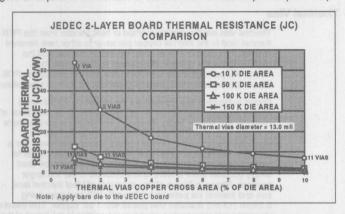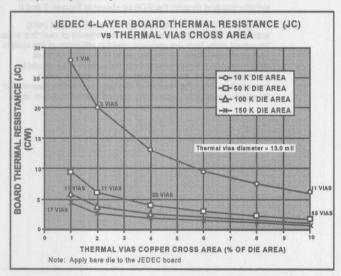
Figure 9. Impact of the Number of 0.33mm (0.013 inch) Diameter Thermal Vias versus Chip Area (Die Area)

JEDEC 4-LAYER BOARD THERMAL RESISTANCE (JC)
vs THERMAL VIAS CROSS AREA

Note: Apply bare die to the JEDEC board
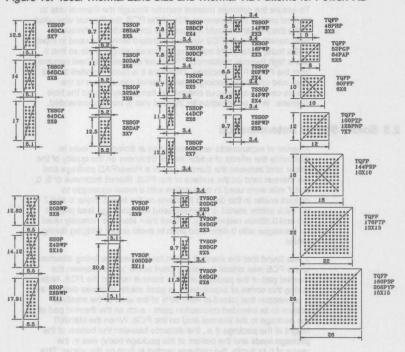
16   SLMA002

Figure 10. Ideal Thermal Land Size and Thermal Via Patterns for PowerPAD

Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0.33mm (13 mils) or smaller works well when 1 ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias will not be plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0.1mm minimum. This will prevent the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.

PowerPAD Thermally Enhanced Package 17

To assure the optimum thermal transfer through the thermal vias to internal planes or the reverse side of the PCB, the thermal vias used in the thermal land should *not* use web construction techniques. Web construction on PCB vias is a standard technique used in most PCBs today to facilitate soldering, by constructing the via so that it has a high thermal resistance. This is *not* desirable for heat removal from the PowerPAD package. Therefore it is recommended that all vias used under the package make internal connections to the planes using a continuous connection completely around the hole diameter. Web construction for thermal vias is not recommended.

2.5 Solder Stencil Determination

A series of experiments were conducted at Solectron-Texas to determine the effects of solder stencil thickness on the quality of the solder joint between the thermal pad of a PowerPAD package and the thermal land on the surface of the PCB. Stencil thickness of 5, 6, and 7 mils were used in conjunction with a metal squeegee to deposit solder in the desired locations on the board. Note: 6 and 7 mil thick solder stencil is normally used with package lead pitch of 0.5 and 0.65mm respectively. A 5 mil thick stencil is normally used for packages with 0.4mm lead pitch to avoid solder bridging during reflow.

It was found that the standoff height for the package being attached to the PCB was critical in making good solder joints between the thermal pad of the package and the thermal land on the PCB. Note: during this series of experiments, a good solder joint was defined as a connection that joined at least 90% of the area of the smallest pattern to its intended connection point - such as the thermal pad of the package to the thermal land on the PCB. When the standoff height of the package (i.e., the distance between the bottom of the package leads and the bottom of the package body) was in the range of 0 to 2 mils, the package tended to float on the solder. This led to the possibility that all leads of the package would not be soldered to the lead traces on the board. This happened even when the 5 mil thick stencil was utilized. There were also cases when the solder was squeezed out from the desired land area, and then formed solder balls during the reflow process - an undesirable result that could cause shorting between package leads on the board surface, or short the thermal land on the PCB to the lead traces. A standoff height of 2.0 to 4.2 mils provided good solder joints for both the leads and the thermal pad for stencil thickness of 5, 6, and 7 mils. When the standoff height of the package was between 4.2 and 6.0 mils, only the 6 and 7 mil thick stencil provided consistently good solder joints for both the package leads and the thermal-pad to thermal-land bond. A general guideline would be to use the thickest solder stencil that works well for the products being assembled for the most process margin in assembling thermally enhanced parts to a PCB.

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The Joint Electron Devices Engineering Council (JEDEC) specification for the standoff height of TSSOP and TQFP packages is the range of 0.05 to 0.15mm (1.97 to 5.91 mils), and is an acceptable range when the solder stencil thickness of 6 and 7 mils are used. Texas Instruments has elected to center the stand-off height of the PowerPAD packages at 3.5 mils (within the JEDEC specification range) to provide good package to PCB solder joint characteristics for standard solder stencil thickness of 5, 6, and 7 mils - the most common range within industry practice today.

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5–161

3. Assembly

Solder joint inspection in the attachment area of the thermal pad of the thermally enhanced packages to the thermal land on the PCB is difficult to perform with the best option to date being x-ray inspection. Tests performed within Texas Instruments and during the joint PCB experiments with Solectron-Texas indicate that x-ray inspection will allow detection of voiding within the solder joint and could be used either in a monitor mode, or for 100% inspection if required by the application. However, this is a slow and costly process so an effort was made to determine the minimum amount of solder required in this joint before degradation of the thermal performance became significant.
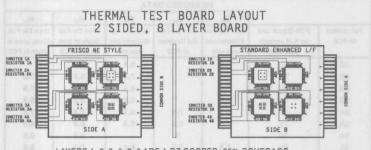
The experimental vehicle used in determining the amount of solder required was a 6S2P double sided test board with copper thermal lands on the surface of the board representing 0%, 7.5%, 22%, and 83% of the package body area. The package used was a 100 pin PowerPAD package (side B - standard enhanced I/f side of the PCB) as shown in Figure 11. There was additional copper area on the surface of the A side of the board due to connections between selected pins and the thermal land area. Four thermal vias were created in each thermal land area with connections to the internal power or ground plane, and continuing to make connection to the thermal land on the opposite side of the board.

A thermal test chip (Texas Instruments x-1158240) with dimensions of 6.1mm (0.240-inch) square was assembled in the test packages using die pad sizes of 6.0mm square, and 9.0mm square. The assembled units were then mounted to the PCB using either eutectic Sn63:Pb37 solder or thermally conductive epoxy adhesive. Measurement of the thermal resistance junction-to-case and thermal resistance junction-to-ambient with the individual packed parts powered at 2.5 watts was made using standard techniques for these measurements. Results are shown in Table 1 for tests with and without attachment between the package thermal pad and the board thermal land, as well as a comparison between solder and thermally conductive epoxy attachment. Table 2 provides the effective connection area obtained for each of the measurement points.

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Figure 11. Test Board for Measurement of Θ_{jc} and Θ_{ja} Using 100 pin PowerPAD TQFP Packages

THERMAL TEST BOARD LAYOUT
2 SIDED, 8 LAYER BOARD

LAYERS 1, 2, 3, 6, 7, 8 ARE 1 OZ COPPER, 20% COVERAGE
LAYERS 4, 5 ARE 1 OZ COPPER, 80% COVERAGE
VIAS IN BOARD CONNECT COMMONS FROM TOP TO LAYERS 4 AND 5
ANTICIPATED POWER LEVEL OF 2.5 WATT MAX FOR EACH PART
STANDARD THERMAL TEST BOARD DIMENSIONS
CONNECTOR IS 0.125 INCH PITCH, 18 CONTACTS/SIDE, 2 SIDES
PACKAGE IS LQFP/TQFP 14 X 14 X 1.0 OR 1.4mm BODY SIZE; 0.5mm LEAD PITCH
VENDOR = SERIUS SOLUTIONS (RAY MULLINS 404-9748) NUMBER 10-00001-00 8 LAYER; K FACTOR X 8; 100 LQFP/TQFP

The relative thermal land size and location is shown along with the location of the thermal vias that connect the surface thermal land to the internal power or ground plane, and continuing to connect to the thermal land on the opposite side of the board. The board is approximately 82.5mm (3.25 inch) square.

Table 2 and Table 3 show the thermal resistance data for Θ_{jc} and Θ_{ja} (junction to case, and junction to ambient) for the 8 layer thermal test board, with the copper thermal land on the PCB shown as a percentage of the area of the package body.

Table 2. Measured Θ_{jc} from Test Board

		MEASURED DATA				
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	9.3		9.9	11.4	
4B	7.5			7.2	5.8	7.2
2B	22	6.8		6.3	7.2	7.5
3B	83	6.2		6.2	6.2	6.2
2A	0	8.7	7.4	9.1	7.8	7.8
3A	7.5	7.6	8.3	6.3	6.8	6.8
1A	30		8		6.6	6.5
4A	85	7.5	7.3	6.4	6.4	6.9

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 3. Measured Θ_{ja} from Test Board

		MEASURED DATA				
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	33.8		40.6	44.3	
4B	7.5			27	23.1	25.5
2B	22	28.4		25.8	25	24.3
3B	83	24.2		26.9	24.6	24
2A	0	34.4	34	33.3	32.3	25.8
3A	7.5	33.5	33	24.4	24.9	25.2
1A	30		31		24.4	23.2
4A	85	33.3	30	25.5	24.6	24

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

Small changes in the percentage of copper land area (between the "A" side of the PCB and the "B" side of the PCB) do not significantly affect the thermal resistance.

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Table 4 and Table 5 show the relationship of the solder joint area between the thermal pad in the PowerPAD package and the thermal land of the PCB for the thermal resistance values obtained in Table 2 and Table 3.

Table 4. *Relationship of the Solder Joint Area on Θ_{jc}, from Test Board Data*

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %					
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Position on PCB	PCB Copper land size on PCB	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	0
4B	4*(2x2)	**36**	16	**16**	**16**	100
2B	1*(6x6)	**80**	32	**32**	**32**	100
3B	1*(12x12)	**100**	100	**100**	**100**	100
2A	0	**0**	0	**0**	**0**	0
3A	4*(2x2)	**80**	16	**16**	**16**	100
1A	1*(6x6)+4*(5.7)	**85**	58	**58**	**58**	100
4A	1*(12x12)+4*(5.6)	**100**	100	**100**	**100**	100

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 5. *Relationship of the Solder Joint Area on Θ_{ja}, from Test Board Data*

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %					
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	0
4B	4*(2x2)	**36**	16	**16**	**16**	100
2B	1*(6x6)	**80**	32	**32**	**32**	100
3B	1*(12x12)	**100**	100	**100**	**100**	100
2A	0	**0**	0	**0**	**0**	0
3A	4*(2x2)	**80**	16	**16**	**16**	100
1A	1*(6x6)+4*(5.7)	**85**	58	**58**	**58**	100
4A	1*(12x12)+4*(5.6)	**100**	100	**100**	**100**	100

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

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In this example, there is significant improvement in thermal heat removal with solder joint areas as small as 16%, and the thermal removal efficiency as measured by Θ_{jc} and Θ_{ja} are within measurement error tolerance for all solder joint areas greater than 32%.

Based on the measured data for this test board configuration, Texas Instruments recommends a minimum solder joint area of 50% of the package thermal pad area when the part is assembled on a PCB. The results of the PCB assembly study conducted with Solectron-Texas indicate that standard board assembly processes and materials will normally achieve >80% solder joint area without any attempt to optimize the process for thermally enhanced packages. A characterization of the solder joint achieved with a given process should be conducted to assure that the results obtained during testing apply directly to the customer application, and that the thermal efficiency in the customer application is similar to the thermal test board results for the power level of the packaged component. If the heat removal is not at the efficiency desired, then either additional thermal via structures will have to be added to the PCB construction, or additional thermal removal paths will need to be defined (such as direct contact with the system chassis).

An alternative to attaching the thermal pad of the package to the thermal land of the PCB with solder is to use thermally conductive epoxy for the attachment. This epoxy can either be dispensed from the liquid form with a material that will cure during the reflow cycle, or a "B" staged preform that will receive the final cure during the reflow cycle. These materials can be the same as normally used with externally applied heat sinks. When epoxy is used as the attachment mechanism, then the effective attachment area is 100% of the die pad area, and there is some added benefit as thermal transfer to the PCB can occur, even with no copper thermal land at the surface of the PCB.

3.1 Solder Reflow Profile Suggestion

The reflow profile for IR board assembly using the Texas Instruments PowerPAD packages does not have to change from that used with conventional plastic packaged parts. The construction of the package does not add thermal mass, and the only new thermal load is due to the increased solder area between the package thermal pad and the thermal land on the PCB. A typical IR oven profile for fine pitch surface mount packages is shown in Figure 11. for eutectic Sn63:Pb37 solder. Nitrogen purged, convection IR reflow will be advantageous for this part to PCB assembly to minimize the possibility of solder ball formation under the package body.
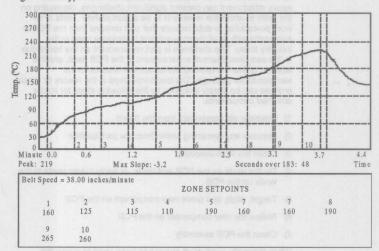
Figure 12 shows a typical infrared (IR) oven profile for a fine pitch plastic package assembly mounted to an FR-4 PCB using eutectic Sn63:Pb37 solder.

Figure 12. Typical Infrared Oven Profile

Belt Speed = 38.00 inches/minute							
			ZONE SETPOINTS				
1	2	3	4	5	6	7	8
160	125	115	110	190	160	160	190
9	10						
265	260						

Peak temperature should be approximately 220 degrees centigrade, and the exposure time should normally be less than 1 minute at temperatures above 183 degrees centigrade.

3.2 Installation and Assembly Summary

The PowerPAD package families can be attached to printed circuit boards using conventional Infrared solder reflow techniques that are standard in the industry today without changing the reflow process used for normal fine pitch surface mount package assembly. A minimum solder attachment area of 50% of the package thermal pad area is recommended to provide efficient heat removal from the semiconductor package, with the heat being carried into or through the PCB to the final thermal management system. This attachment can be achieved either by the use of solder for the joining material, or through the use of thermally conductive epoxy materials. Typical PCB thermal land pattern definitions have been provided that have been shown to work with 4 and 8 layer PCB test boards, and can be extended for use by other board structures.

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4. Repair

Reworking thermally enhanced packaged semiconductors that have been attached to PCB assemblies through the use of solder or epoxy attachment can present significant challenges, depending on the point at which the re-work is to be accomplished. Tests of re-work procedures to date indicate that part removal from the PCB is successful with all of the conventional techniques used in the industry today. The challenge is part replacement on the board due to the combined thermal enhancement of the PCB itself, and the addition of thermal removal enhancement features to the semiconductor package. The traditional steps in the rework or repair process can be simply identified by the following steps for solder attached components:

1) Unsolder old component from the board

2) Remove any remaining solder from the part location

3) Clean the PCB assembly

4) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB

5) Target, align, and place new component on the PCB

6) Reflow the new component on the PCB

7) Clean the PCB assembly

When thermally conductive epoxy has been used to attach the thermal pad of the package to the thermal land on the PCB, the same basic steps in the rework or repair procedure can be followed with only minor modifications:

1) Unsolder old component and torque package to remove from the board

2) Remove any remaining solder from the part location

3) Remove any remaining epoxy from the thermal land on the PCB

4) Clean the PCB assembly

5) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB

6) Place new thermally conductive "B" staged epoxy preform or dispense epoxy on thermal land

7) Target, align, and place new component on the PCB

8) Reflow the new component on the PCB

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9) Complete epoxy cure (if required as a separate step)

10) Clean the PCB assembly

4.1 Part Removal From PCBs

Almost any removal process will work to remove the device from the PCB, even with the thermal pad of the package soldered to the PCB. Heat is easily transferred to the area of the solder attachment either from the exposed surface thermal land of the PCB (single layer example), or through the thermal vias in the PCB (multi-layer example) from the backside of the PCB.

Re-work has been performed for both the TSSOP and TQFP PowerPAD style packages using METCAL removal irons and hot air. The specific example of a 20 pin TSSOP PowerPAD part removal is discussed in detail.

A 750-Watt METCAL removal iron was used in conjunction with hot air to verify the removal method efficiency to take 20 pin PowerPAD TSSOP packages off of assembly test boards. The hot air method is recommended as it subjects the PCB and surrounding components to less thermal and mechanical stress than other methods available, and has been proven to be much easier to control than some of the hot bar techniques. Use of the hot air method may require assemblers to acquire tools specifically for the smaller packages since most assemblers use a hot bar method for packages of this size. (Note: This same tool will also be needed for part re-attachment to the PCB when the hot air method is employed). A tool with an integrated vacuum pick up tip will be an advantage in the part removal process so the part can be physically removed from the board as soon as the solder reaches liquidus. Preheating of the local area of the PCB to a temperature of approximately 160 degrees centigrade can make the part removal easier. This is especially helpful in the case of larger packages such as 56 pin TSSOP or 100-pin TQFP style packages. This preheat will be required in the thermal removal method if the semiconductor package is a heat slug package rather than the TI PowerPAD package version. Some experimentation will be required to find the optimum procedure to use for any specific PCB construction and thermally enhanced package version.

After the part has been removed from the PCB, conventional techniques to clean the area of the part attachment - such as solder wicking - will be needed to prepare the location for subsequent attachment of a new component.

When thermally conductive epoxy has been used for attachment of the package thermal pad to the thermal land on the PCB, a slightly different approach to part removal must be used. This will require a tool that has dimensions that will allow contact with the sides of the package body directly above the leads, and will allow the package to be twisted or rotated horizontally when the solder joints of the package leads have reached liquidus. The temperature at the epoxy interface to the package thermal pad or the PCB thermal land must be above the glass transition temperature of the epoxy (typically less than 180 degrees centigrade) to break the adhesion between the epoxy and the attach location with the twisting or rotational method discussed above. In most cases, any remaining epoxy on the PCB after part removal can be removed by peeling it from the surface - occasionally, it will be necessary to apply heat to the epoxy location so it will peel away from the PCB cleanly.

4.2 Attachment of a Replacement Component to the PCB

Preparation of the PCB for attachment of a new component follows normal industry practice with respect to the lands on the board and the leads of the package. Both may be tinned, and/or solder paste applied to the lands for new component attachment. In addition, when solder will be used to re-attach the thermal pad of the package to the thermal land on the PCB, solder paste will need to be applied to the surface of the thermal land on the board. This may be in the form of stripes of solder paste with sufficient volume to achieve the desired solder coverage, or a solder preform may be applied to the location for attachment. In a factory environment, the component is then placed in the desired location and alignment, and processed through a reflow oven to re-establish the desired solder joints. This is the most desirable process and is normally the easiest to accomplish.

When a manual or off-line attachment and reflow procedure is to be used, the challenge of supplying sufficient heat to the components and solder becomes a greater concern. In most cases, the corner leads of the package being attached will be tack soldered to hold the component in alignment so the balance of the leads and the thermal pad to thermal land solder reflow can be accomplished without causing part movement from its desired location. As in the part removal case, it is advisable to pre-heat the board or the specific device location to a temperature below the melting point of the solder to minimize the amount of heat that must be provided by the reflow device as the part is being attached. A good starting point is to pre-heat to approximately 160 degrees centigrade. A hot gas reflow tool can then be used to complete the solder joint formation both at the leads and for the connection of the thermal pad to the thermal land of the PCB. Care must be taken at this operation to avoid blowing solder out from the thermal pad to thermal land interface and causing solder balling under the package or creating

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lead to lead or thermal land to lead shorts. The thermal enhancement of the package and the PCB will require a higher temperature gas or higher gas flow to reach solder liquidus than would be needed with an assembly lacking these enhancements. The tool should be specifically sized to the part being reworked to minimize possible damage to surrounding components or the PCB itself.

If the re-attachment of the interface between the thermal pad of the package and the thermal land of the PCB using solder attachment is too difficult to control using hot gas methods, then the best approach is to use either a thermally conductive "B" staged epoxy preform cut to the shape of the thermal land on the PCB, or dispensing liquid thermally conductive epoxy in a pattern on the thermal land that will result in at least a 50% void free connection between the pad and the land. Virtually any epoxy material that is used for the attachment of external heat sinks to packaged components is suitable for this application, and cure time/temperature requirements can be matched to the product need (anywhere from 24 hours at room temperature to less than 1 hour at temperatures below 100 degrees centigrade). Care must be taken to choose a material with limited run-out to avoid the possibility of shorting adjacent package leads together or shorting the thermal land of the PCB to the package leads.

It should be noted that the Texas Instruments PowerPAD packages are easier to rework at the board level than other semiconductor packages utilizing metal slugs for the thermal path between the chip and the PCB. This is due to the additional requirement for heating the total mass of the slug to reflow temperatures versus heating the thermal pad of the PowerPAD package. The hot gas temperature and/or flow becomes critical for effective joining of the components without causing damage to the adjacent components or the PCB. In either case, the use of thermally conductive epoxy materials will make the rework task easier and more reliable to perform in a manual repair environment.

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5. Summary

An overview of the design, use and performance of the Texas Instruments PowerPAD package has been presented. The package is simple to use and can be assembled and repaired using existing assembly and manufacturing tools and techniques. Package performance is outstanding. By exposing the leadframe on the package bottom, extremely efficient thermal transfer between the die and the PCB can be achieved.

The simplicity of the PowerPAD package not only makes for a low cost package, but there is no additional cost in labor or material for the customer using standard surface mount assembly techniques. The only preparation needed to implement a PowerPAD design is at the PCB design stage. Simply by including a thermal land and thermal vias on the PCB the design can use the PowerPAD package effectively.

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Appendix A. Thermal Modeling of PowerPAD Packages

Table 6. Thermal Characteristics for Different Package and PCB Configurations

Package Description			2 oz. Trace and Copper Pad with Solder			2 oz. Trace and Copper Pad without Solder			Standard Package JEDEC Low Effect with 1 oz. trace		
Pkg Type	Pin Count	Package Designator	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)
SSOP	20	DWP	21.46	0.37	1.617	43.91	0.37	6.031	92.95	16.58	2.212
	24	DWP	20.77	0.27	1.507	38.43	0.27	4.88	80.49	13.49	1.959
	28	DWP	19.52	0.22	1.337	33.92	0.22	4.109	69.73	11.24	1.641
TVSOP	80	DDP	19.88	0.21	0.196	32.64	0.21	0.359	65.53	4.69	0.353
	100	DDP	18.35	0.17	0.182	28.45	0.17	0.313	54.55	3.73	0.297
	20	DGP	37.92	2.46	1.074	95.88	2.46	3.318	192.65	28.85	1.054
	24	DGP	36.87	2.46	1.056	89.50	2.46	3.176	179.91	28.41	0.999
	48	DGP	27.35	0.72	0.45	52.82	0.72	1.138	107.49	12.32	0.58
	56	DGP	25.42	0.58	0.406	46.69	0.58	0.98	95.48	10.40	0.526
TSSOP	48	DCA	22.30	0.32	0.22	40.27	0.32	0.443	84.04	6.63	0.434
	56	DCA	21.17	0.27	0.212	36.42	0.27	0.401	75.50	5.81	0.395
	64	DCA	19.89	0.21	0.196	32.52	0.21	0.357	65.70	4.69	0.35
	28	DAP	25.10	0.45	0.244	51.28	0.45	0.556	110.60	8.96	0.548
	30	DAP	24.20	0.45	0.233	48.34	0.45	0.551	103.45	8.73	0.486
	32	DAP	23.51	0.32	0.233	44.32	0.32	0.468	95.63	7.32	0.478
	38	DAP	22.41	0.31	0.219	41.18	0.31	0.444	87.32	6.57	0.454
	28	DCP	30.62	0.94	0.534	63.99	0.94	1.424	133.67	16.13	0.707
	30	DCP	30.55	0.94	0.532	63.32	0.94	1.408	131.23	16.05	0.695
	38	DCP	27.41	0.72	0.447	52.93	0.72	1.13	109.55	12.42	0.598
	44	DCP	25.57	0.58	0.406	47.18	0.58	0.982	97.13	10.47	0.538
	50	DCP	24.10	0.51	0.369	43.76	0.51	0.892	89.53	9.34	0.5
	14	PWP	37.47	2.07	0.851	97.65	2.07	2.711	195.35	26.86	1.047
	16	PWP	36.51	2.07	0.848	90.26	2.07	2.6	182.31	26.56	0.964
	20	PWP	32.63	1.40	0.607	74.41	1.40	1.777	151.89	19.90	0.77
	24	PWP	30.13	0.92	0.489	62.05	0.92	1.263	128.44	14.83	0.665
	28	PWP	27.87	0.72	0.446	56.21	0.72	1.169	115.82	12.41	0.623
TQFP	48	PHP	29.11	1.14	0.429	64.42	1.14	1.262	108.71	18.18	0.511
	52	PGP	21.61	0.38	0.192	42.58	0.38	0.391	77.15	7.83	0.353
	64	PBP	17.46	0.12	0.155	28.04	0.12	0.252	52.21	3.12	0.267
	64	PAP	21.47	0.38	0.19	42.20	0.38	0.386	75.83	7.80	0.347
	80	PFP	19.04	0.17	0.174	31.52	0.17	0.29	57.75	4.20	0.297
	100	PZP	17.28	0.12	0.154	27.32	0.12	0.247	49.17	3.11	0.252
	128	PNP	17.17	0.12	0.152	27.07	0.12	0.244	48.39	3.11	0.248
LQFP	144	PRP	15.68	0.13	0.199	27.52	0.13	0.346	47.34	4.62	0.288
	176	PTP	14.52	0.10	0.17	24.46	0.10	0.28	42.95	3.67	0.257
	160	PSP	11.14	0.10	0.14	22.40	0.10	0.266	43.93	3.70	0.262
	208	PYP	10.96	0.10	0.139	21.48	0.10	0.258	39.18	3.66	0.235

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General

Thermal modeling is used to estimate the performance and capability of IC packages. From a thermal model, design changes can be made and thermally tested before any time is spent on manufacturing. It can also be determined what components have the most influence on the heat dissipation of a package. Models can give an approximation of the performance of a package under many different conditions. In this case, a thermal analysis was performed in order to approximate the improved performance of a PowerPAD thermally enhanced package to that of a standard package.

Modeling Considerations

There are only a few differences between the thermal models of the standard packages and models for PowerPAD. The geometry of both packages was essentially the same, except for the location of the lead frame bond pad. The pad for the thermally enhanced PowerPAD package is deep downset, so its location is further away from the lead fingers than a standard package lead frame pad. Both models used the maximum pad and die size possible for the package, as well as using a lead frame that had a gap of one lead frame thickness between the pad and the lead fingers. The lead frame thickness was:

      TQFP/LQFP: 0.127 mm, or 5 mils
      TSSOP/TVSOP/SSOP: 0.147 mm, or 5.8 mils

In addition, the board design for the standard package is different than the PowerPAD. One of the most influential components on the performance of a package is board design. In order to take advantage of PowerPAD's heat dissipating abilities, a board must be used that acts similarly to a heat sink and allows for the use of the exposed (and solderable) deep downset pad. This is Texas Instruments' recommended board for PowerPAD (see

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Figure 13). A summary of the board geometry is included below.

Texas Instruments Recommended Board for PowerPAD

0.062" thick

3" x 3" (for packages <27 mm long)

4" x 4" (for packages >27 mm long)

2 oz. copper traces located on the top of the board (0.071 mm thick)

Copper areas located on the top and bottom of the PCB for soldering

Power and ground planes, 1 oz. copper (0.036 mm thick)

Thermal vias, 0.33 mm diameter, 1.5 mm pitch
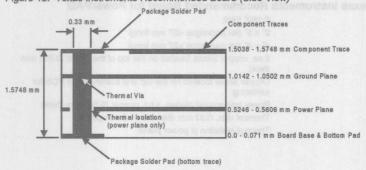
Thermal isolation of power plane

Figure 13. Texas Instruments Recommended Board (Side View)

The standard packages were placed on a board that is commonly used in the industry today, following the JEDEC standard. It does not contain any of the thermal features that are found on the Texas Instruments recommended board. It only has component traces on the top of the board. A summary of the standard is located below:

JEDEC Low Effective Thermal Conductivity Board (Low-K)

0.062" thick

3" x 3" (for packages <27 mm long)

4" x 4" (for packages >27 mm long)

1 oz. copper traces located on the top of the board (0.036 mm thick)

These boards were used to estimate the thermal resistance for both PowerPAD and the standard packages under many different conditions. While the PowerPAD can be used on a JEDEC low-k board, in order to achieve the maximum thermal capability of the package, it is recommended that it be used on the Texas Instruments heat dissipating board design. It allows for the exposed pad to be directly soldered to the board, which creates an extremely low thermal resistance path for the heat to escape.

A general modeling template was used for each PowerPAD package, with variables dependent on the package size and type. The package dimensions and an example of the template used to model the packages are shown in Figure 14 and Table 7. While only 1/4 of the package was modeled (in order to simplify the model and to lessen the calculation time), the dimensions shown are those for a full model.

Figure 14. Thermal Pad and Lead Attachment to a PCB Using the PowerPAD Package
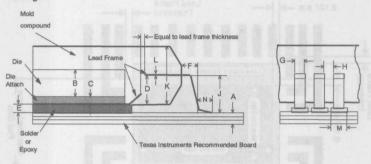
Table 7. PowerPAD Package Template Description

(A)	PCB Thickness:	1.5748 mm	(K)	Package Thickness:	(3)
	PCB Length:	76.2 mm (1)		Package Length:	(3)
	PCB Width:	76.2 mm (1)		Package Width:	(3)
(B)	Chip Thickness:	0.267 mm	(L)	Pad Thickness:	0.147 mm (8)
	Chip Length:	(2)		Pad Length:	(3)
	Chip Width:	(2)		Pad Width:	(3)
(C)	Die Attach Thickness:	0.0127 mm		PCB Trace Length:	25.4 mm
(D)	Lead Frame Downset:	(3)		PCB Trace Thkn:	0.071 mm
	Tie Strap Width:	(3)		PCB Backplane Th:	0.0 mm (4)
(E)	PCB to Package Bottom:	0.09 mm		PCB Trace Width:	0.254 mm
(G)	Shoulder Lead Width:	(3),(5),(6)	(M)	Foot Width:	(5)
(H)	Shoulder Lead Space:	(3),(6)	(N)	Foot Length on PCB:	(3)
(J)	Shoulder to PCB Dist.:	(7)			

Notes: 1) 99.6mm for packages > 27mm max length
   2) Chip size is 10 mils smaller than the largest pad size (5 mils from each side)
   3) Dependent on package size and type
   4) The recommended board requires the addition of two internal copper planes, solder pads, and thermal vias
   5) Foot width was set equal to shoulder lead width for model efficiency
   6) Lead pitch is equal to the shoulder lead width plus the shoulder lead space (pitch = G + H)
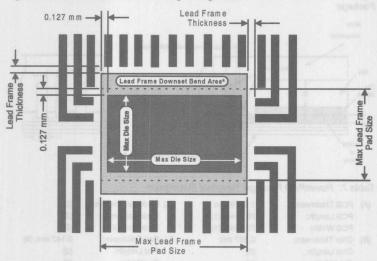
7) The shoulder to board distance is equal to the downset plus the board to package bottom distance (J = D + E)
8) The pad thickness for TQFP/LQFP is equal to 0.127 mm
9) All dimensions are in millimeters.

In addition to following a template for the dimensions of the package, a simplified lead frame was used. A description of the lead frame geometry is seen in Figure 15.

Figure 15. General Leadframe Drawing Configuration

NOTE:
The lead frame downset bend area = 20 mils (lead frame thickness). For SSOP, TSSOP, and TVSOP packages, add the bend area to the width of the pad. For TQFP and LQFP, add the bend area to both the width and length of the pad.

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Results

The purpose of the thermal modeling analysis was to estimate the increase in performance that could be achieved by using the PowerPAD package over a standard package. For this package comparison, several conditions were examined:

Case 1. PowerPAD soldered to the TI recommended board

Case 2. PowerPAD not soldered to the TI recommended board
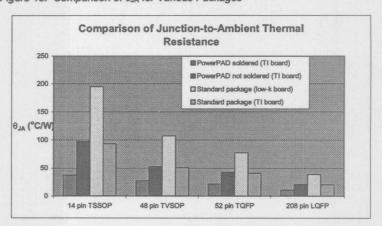
Case 3. A standard package configuration on a low-k board

Case 4. A standard package on the TI recommended board

The first three cases show a comparison of PowerPAD packages on the recommended board to standard packages on a board commonly used in the industry. The results are shown in Table 6. From these results, it was shown that the PowerPAD, when soldered to the TI recommended board, performed an average of 47% cooler than when not soldered, and 73% cooler than a standard package on a low-k board.

For the final case, a separate analysis was performed in order to show the difference in thermal resistance when the standard and the thermally enhanced packages are used on the same board. The results showed that the PowerPAD, when soldered, performed an average of 44% cooler than the standard package (See Figure 18).

Figure 18. Comparison of θ_{JA} for Various Packages

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However, when the PowerPAD is not soldered to the board, similar to a standard package, the θ_{JA} is approximately 3% hotter than a standard package. This is due to the location of the lead frame pad relative to the lead fingers, which is the strongest conduction path in a standard package. Since the pad on a standard package lead frame is closer to the lead fingers, more heat is dissipated through the leads than in the PowerPAD package with its deep downset pad.

Conclusions

The deep downset pad of a PowerPAD package allows for an extensive increase in package performance. Standard packages are limited by using only the leads to transport a majority of the heat away. The addition of a heat sink will improve standard package performance, but greatly increases the cost of a package. The PowerPAD package improves performance, but maintains a low cost. The results of the thermal analysis showed that by soldering the PowerPAD package directly to a board designed to dissipate heat, thermal performance increased approximately 44% over the standard packages used on the same board.

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Figure 18. Comparison of θ_JA for Various Packages

However, when the PowerPAD is not soldered to the board, similar to a standard package, the θ_JA is approximately 3% hotter than a standard package. This is due to the location of the lead frame pad relative to the lead fingers, which is the strongest conduction path in a standard package. Since the pad on a standard package lead frame is closer to the lead fingers, more heat is dissipated through the leads than in the PowerPAD package with its deep downset pad.

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![TI logo]

Appendix B. Rework Process for Heat Sink TQFP and TSSOP PowerPAD Packages - from Air-Vac Engineering

Introduction

The addition of bottom side heat sink attachment has enhanced the thermal performance of standard surface mounted devices. This has presented new process requirements to effectively remove, redress, and replace (rework) these devices due to the hidden and massive heat sink, coplanarity issues, and balance of heat to the leads and heat sink. The following is based on rework of the TQFP100 and TSSOP20/24 pin devices.

Figure 19. DRS22C Reworking Station

Equipment

The equipment used was the Air-Vac Engineering DRS22C hot gas reflow module. The key requirements for the heat sink applications include: stable PCB platform with sufficient bottom side preheat, alignment capabilities, very accurate heat control, and proper nozzle design.

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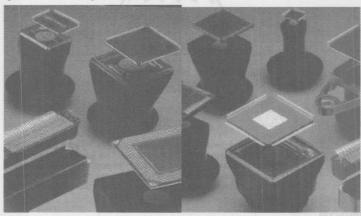
PCB support is critical to reduce assembly sagging and to provide a stable, flat condition throughout the process. The robust convection-based area heater provides sufficient and accurate bottom side heat to reduce thermal gradient, minimize local PCB warpage, and compensate for the heat sink thermal characteristics. The unique pop-up feature allows visible access to the PCB with multiple easy position board supports.
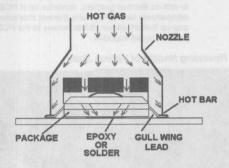
Figure 20. Reworking Nozzles of Various Sizes

During removal, alignment, and replacement, the device is held and positioned by a combination hot gas/hot bar nozzle. Built-in nozzle tooling positions the device correctly to the heat flow. A vacuum cup holds the component in place. Hot gas is applied to the top of the device while hot gas/hot bar heating is applied to the component leads. The hot bar feature also insures bonding of the fine pitch leads.

Figure 21. Nozzle Configuration

Profile

The gas temperature, flow, and operator step-by-step instructions are controlled by an established profile. This allows complete process repeatability and control with minimal operator involvement. Very accurate, low gas flow is required to insure proper temperature control of the package and to achieve good solder joint quality.

Removal

The assembly is preheated to 75 °C. While the assembly continued to preheat to 100 °C, the nozzle is preheated. After the preheat cycle, the nozzle is lowered and the device is heated until reflow occurs. Machine settings: TSSOP 20/24 - 220 °C at 0.39 scfm gas flow for 50 seconds (preheat) above board level, 220 °C at 0.39 scfm for 10 seconds. TQFP 100 - 240 °C at 0.10 scfm for 60 seconds (preheat) above board level, 250 °C at 0.65 scfm for 15 seconds. The built in vacuum automatically comes on at the end of the cycle and the nozzle is raised. The time to reach reflow was approximately 15 seconds. The component is released automatically allowing the part to fall into an appropriate holder.

Site Redress

After component removal the site must be cleaned of residual solder. This may be done by vacuum desoldering or wick. The site is cleaned with alcohol and lint-free swab. It is critical that the heat sink area be flat to allow proper placement on the leads on new device. Stenciling solder paste is the preferred method to apply new solder. Solder dispensing or reflowing the solder bumps on the pads for the leads may also be an alternative, but reflow (solid mass) of solder to the heat sink is not.

Figure 22. Air-Vac Vision System

Alignment

A replacement device is inserted into the gas nozzle and held by vacuum. The device is raised to allow the optical system to be utilized. The optical system used for alignment consists of a beam-splitting prism combined with an inspection quality stereo microscope or camera/video system. the leads of the device are superimposed over the corresponding land pattern on the board. This four sided viewing allows quick and accurate operator alignment.

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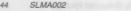
Replacement

Once aligned, the x/y table is locked and the optical system retracts away from the work area. The preheat cycle is activated. The device is then lowered to the board. An automatic multi-step process provides a controlled reflow cycle with repeatable results. Machine settings for TSSOP 20/24: 160 °C at 0.39 scfm gas flow for 40 seconds (preheat), 220 °C at 0.39 scfm for 60 seconds above board level, 220 °C at 0.39 scfm for 10 seconds. For TQFP 100: 100 °C at 0.78 scfm for 40 seconds (preheat), 240 °C at 0.10 scfm for 90 seconds above board level, 250 °C at 0.65 scfm for 15 seconds (2 stages).

Conclusion

Rework of heat sink devices, TQFP and TSSOP, can be successful with attention to the additional issues they present. With respect to proper thermal profiling of the heat sink, die, and lead temperatures, the correct gas nozzle and profile can be developed to meet the requirements of the device and assembly. Existing equipment and nozzle design by Air-Vac can provide the tools and process knowledge to meet the heat sink TQFP and TSSOP rework application.

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Appendix C.   PowerPAD Process Rework Application Note from Metcal

The following report references six of Texas Instruments' fine pitch, surface mount prototype packages (TSOP20, TSOP56, TSOP24, TQFP100, and TQFP64). The shapes and sizes are not new to the circuit board industry. Normally, I would use Metcal conduction tools to simply remove and replace these components. However, these packages are unique because all packages include a 'dye lead' on the underside of the package. This dye lead cannot be accessed by contact soldering. Therefore, convection rework methods are necessary for component placement.

NOTE:

Conduction tools can be used for removal. But, convection rework techniques are required for placement, and recommended for removal.)

Removal

Conduction (optional): All packages can be removed with Metcal conduction tips. Use the following tips:

Component	Metcal Tip Cartridge	OK Nozzle
TSOP20	SMTC-006	N-S16
TSOP56	SMTC-166	N-TSW32
TSOP24	SMTC-006	N-S16
TQFP100	SMTC-0118	N-P68
TQFP64	SMTC-112	N-P20

The dye lead, which is not in contact with the Metcal tip, will easily reflow as heat passes through the package.

Conduction Procedure

1) Tin the tip, contact all perimeter leads simultaneously, and wait 3-5 seconds for the leads to reflow.

2) Lift the package off the board (surface tension will hold it in the tip cartridge). Dislodge the component from the tip by wiping the tip cartridge on a damp sponge.

Convection Procedure

1) Flux the leads. Preferably, use a liquid RMA/rosin flux. Pre-heat the board at 100C. Use a convection or IR preheater, like the SMW-2201 from OK Industries. The settings 2-4 will generally heat a heavy board to 100° in 60 seconds.

PowerPAD Thermally Enhanced Package   45

2) Remove the component with the OK Industries FCR hot air system. Use a nozzle that matches the size and shape of the component (see above). With the preheat still on, heat the top of the board for 30-45 seconds on a setting of 3-4 (depending on board thickness and amount of copper in board*).

Since convection is NECESSARY for placement, convection is recommended for removal.

Placement Procedure

1) Pads can be tinned by putting solder paste on the pads and reflowing with hot air. Simply apply a fine bead of solder paste (pink nozzle, 24AWG) to the rows of pads. Be sure to apply very little paste. Excessive paste will cause bridging, especially with fine pitch components.

2) Once the pads are tinned, apply gel flux (or liquid flux) to the pads. RMA flux is preferable. Be sure to apply gel flux to the dye pad as well. It is important that your pads not be OVER tinned. If too much solder has formed on the dye pad, the component will sit above the perimeter leads, causing co-planarity problems. The gel flux is tacky and helps with manual placement. The joints require very little solder, so stenciling is not necessary. The pads are so thin that a minimal amount of solder is needed to form a good joint. Use a hot air nozzle for the FCR system. Pre-heat the board and (setting 3-5). Use low air flow (5-10 liters/minute) and topside heat (setting 3-4) for about 30-45 seconds*.

NOTES:

The quality of the dye lead's solder joint cannot be visually inspected. An X-ray machine, cross sectioning, or electrical testing will be required.

The vias on the test board are not solder masked very well which causes some bridging and solder wicking.

*Specific board and component temperatures will vary from board to board and from nozzle to nozzle. Larger nozzles require a higher setting because the heat must travel farther away from the heat source. There will be a slight convection cooling effect from pushing hot air through long flutes, and depending on how wide the nozzle is. However, as a rule, keep the board temperature at 100 °C (as thermocoupled from the TOP). You can regulate the board temperature by setting the temperature knob on the bottom side pre-heater. Apply a HIGHER topside heat from the FCR heating head. As a rule, use a maximum of 200-210°C for a short peak period (10 seconds). Look for the flux to burn off. For board profiling purposes, you can visually inspect the condition of the solder joints during the removal process. Note the time allotted for reflow and set the system to Auto Remove or Auto Place at the same time designation for good repeatability. Be sure not to overheat the joints. Excessive heat can cause board delamination and discoloration. Alignment will 'self-correct' once all the solder has reflowed. Tap board lightly. Remove any solder bridges with solder braid. Also, limit the board's heating cycles to a minimum. Excessive heat shock may warp the board or cause cracking in the solder joints.

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Single Supply Op Amp Design Techniques

Application Report

October 1999

Mixed Signal Products

SLOA030

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Single Supply Op Amp Design Techniques

Ron Mancini

ABSTRACT

This application report describes single supply op amp applications, their portability and their design techniques. The single supply op amp design is more complicated than a spilt or dual supply op amp, but single supply op amps are more popular because of their portability. New op amps, such as the TLC247X, TLC07X, and TLC08X have excellent single supply parameters. When used in the correct applications, these op amps yield almost the same performance as their split supply counterparts. The single supply op amp design normally requires some form of biasing.

Introduction

Most portable systems have one battery, thus the popularity of portable equipment results in increased single supply applications. Split or dual supply op amp circuit design is straightforward because the op amp inputs and outputs are referenced to the normally grounded center tap of the supplies. In the majority of split supply applications, signal sources driving the op amp inputs are referenced to ground. Thus with one input of the op amp referenced to ground, as shown in Figure 1, there is no need to consider input common–mode voltage problems.

$$V_{OUT} = -V_{IN} \frac{R_F}{R_G}$$
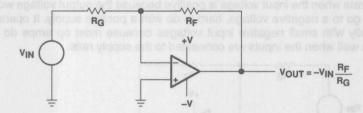
Figure 1. Split Supply Op Amp Circuit

When the signal source is not referenced to ground (see Figure 2), the voltage difference between ground and the reference voltage shows up amplified in the output voltage. Sometimes this situation is okay, but other times the difference voltage must be stripped out of the output voltage. An input bias voltage is used to eliminate the difference voltage when it must not appear in the output voltage (see Figure 3). The voltage, V_{REF}, is in both input circuits, hence it is named a common-mode voltage. Voltage feedback op amps, like those used in this application note, reject common-mode voltages because their input circuit is constructed with a differential amplifier (chosen because it has natural common-mode voltage rejection capabilities).
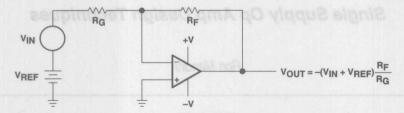
Figure 2. Split Supply Op Amp Circuit With Reference Voltage Input
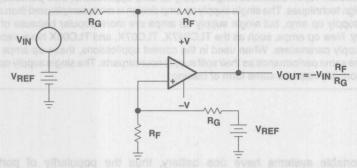
Figure 3. Split Supply Op Amp Circuit With Common-Mode Voltage

When signal sources are referenced to ground, single supply op amp circuits exhibit a large input common-mode voltage. Figure 4 shows a single supply op amp circuit that has its input voltage referenced to ground. The input voltage is not referenced to the midpoint of the supplies like it would be in a split supply application, rather it is referenced to the lower power supply rail. This circuit does not operate when the input voltage is positive because the output voltage would have to go to a negative voltage, hard to do with a positive supply. It operates marginally with small negative input voltages because most op amps do not function well when the inputs are connected to the supply rails.
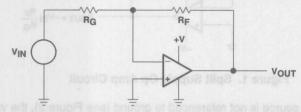
Figure 4. Single Supply Op Amp Circuit

When the signal source is not referenced to ground (see Figure 3), the voltage difference between the input voltage and the reference voltage is amplified in the output voltage. Sometimes this situation is okay, but other times the difference voltage must be stripped out of the output voltage. An input bias voltage is used to eliminate the difference voltage when it must not appear in the output voltage (see Figure 3). The voltage, V_{REF}, is in both input circuits, hence it is named a common-mode voltage. Voltage feedback op amps, like those used in this application, reject common-mode voltages because their input circuit is constructed with a differential amplifier (chosen because it has natural common-mode voltage rejection capabilities).

The constant requirement to account for inputs connected to ground or other reference voltages makes it difficult to design single supply op amp circuits. This application note develops an orderly procedure which leads to a working design every time. If you do not have a good working knowledge of op amp equations, please reference the *Understanding Basic Analog....* series of application notes available from Texas Instruments. Application note SLAA068 titled, *Understanding Basic Analog-Ideal Op Amps* develops the ideal op amp equations. Circuit equations are written with the ideal op amp assumptions as specified in *Understanding Basic Analog–Ideal Op Amps*; the assumptions are tabulated below for your reference.

PARAMETER NAME	PARAMETERS SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

Unless otherwise specified, all op amps circuits are single supply circuits. The single supply may be wired with the negative or positive lead connected to ground, but as long as the supply polarity is correct, the wiring does not affect circuit operation.

Boundary Conditions

Use of a single supply limits the polarity output voltage. For example, when the supply voltage, V_{CC}, = 10 V the output voltage is limited to the range $0 \leq V_{out} \leq 10$. This limitation precludes negative output voltages when the circuit has a positive supply voltage, but it does not preclude negative input voltages when the circuit has a positive supply voltage. As long as the voltage on the op amp input leads does not become negative, the circuit can handle negative input voltages.

Beware of working with negative (positive) input voltages when the op amp is powered from a positive (negative) supply because op amp inputs are highly susceptible to reverse voltage breakdown. Also, insure that all possible start-up conditions do not reverse bias the op amp inputs when the input and supply voltage are opposite polarity.

Circuit Analysis

The first circuit to be examined is the inverting circuit shown in Figure 5.
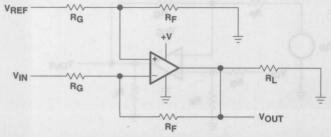
Figure 5. Inverting Op Amp

Equation 1 is written with the aid of superposition, and simplified algebraically, to acquire equation 2.

$$V_{OUT} = V_{REF}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{R_F + R_G}{R_G}\right) - V_{IN}\frac{R_F}{R_G} \tag{56}$$

$$V_{OUT} = \left(V_{REF} - V_{IN}\right)\frac{R_F}{R_G} \tag{57}$$

As long as the load resistor, R_L, is a large value, it does not enter into the circuit calculations, but it can introduce some second order effects which might show up in the lab. Equation 3 is obtained by setting V_{REF} equal to V_{IN}, and there is no output voltage from the circuit regardless of the input voltage. The author unintentionally designed a few of these circuits before he created an orderly method of op amp circuit design. Actually, a real circuit has a small output voltage equal to the lower transistor saturation voltage, which is about 150 mV for a TLC07X.

$$V_{OUT} = \left(V_{REF} - V_{IN}\right)\frac{R_F}{R_G} = \left(V_{IN} - V_{IN}\right)\frac{R_F}{R_G} = 0 \tag{58}$$

When $V_{REF} = 0$, $V_{OUT} = -V_{IN}(R_F/R_G)$, there are two possible solutions to equation 2. First, when V_{IN} is any positive voltage, V_{OUT} should be negative voltage. The circuit can not achieve a negative voltage with a positive supply, so the output saturates at the lower power supply rail. Second, when V_{IN} is any negative voltage, the output spans the normal range according to equation 5.

$$V_{IN} \geq 0, \qquad V_{OUT} = 0 \tag{59}$$

$$V_{IN} \leq 0, \qquad V_{OUT} = |V_{IN}|\frac{R_F}{R_G} \tag{60}$$

When V_{REF} equals the supply voltage, V_{CC}, we obtain equation 6. When V_{IN} is positive V_{OUT} should exceed V_{CC}; that is impossible, so the output saturates. When V_{IN} is negative the circuit acts as an inverting amplifier.

$$V_{OUT} = \left(V_{CC} - V_{IN}\right)\frac{R_F}{R_G} \tag{61}$$

The transfer curve for the circuit shown in Figure 6 (V_{CC} = 5 V, $R_G = R_F$ = 100 K, R_L = 10K) is shown in Figure 7.
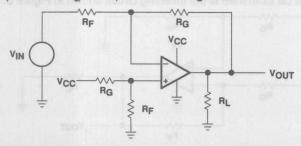
Figure 6. Inverting Op Amp With V_{CC} Bias
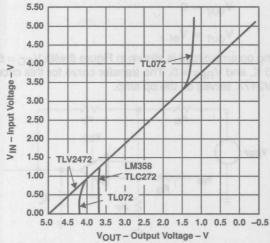
Figure 7. Transfer Curve for Inverting Op Amp With V_{CC} Bias

Four op amps were tested in the circuit configuration shown in Figure 6. Three of the old generation op amps, LM358, TL07X, and TLC272 had output voltage spans of 2.3 to 3.75 volts. This performance does not justify the ideal op amp assumption that was made in the beginning of this application note unless the output voltage swing is severely limited. Limited output or input voltage swing is one of the worst deficiencies a single supply op amp can have because the limited voltage swing limits the circuit's dynamic range. Also, limited voltage swing frequently results in distortion of large signals. The fourth op amp tested was the newer TLV247X which was designed for rail-to-rail operation in single supply circuits. The TLV247X plotted a perfect curve (results limited by the instrumentation), and it amazed the author with a textbook performance that justifies the use of ideal assumptions. Some of the older op amps must limit their transfer equation as shown in equation 7.

$$V_{OUT} = \left(V_{CC} - V_{IN}\right)\frac{R_F}{R_G} \quad \text{for} \quad V_{OUTLOW} \leq V_{OUT} \leq V_{OUTHI} \tag{62}$$

The noninverting op amp circuit is shown in Figure 8. Equation 8 is written with the aid of superposition, and simplified algebraically, to acquire equation 9.

$$V_{OUT} = V_{IN}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{R_F + R_G}{R_G}\right) - V_{IN}\frac{R_F}{R_G} \tag{63}$$

$$V_{OUT} = \left(V_{IN} - V_{REF}\right)\frac{R_F}{R_G} \tag{64}$$

When $V_{REF} = 0$, $V_{OUT} = V_{IN}\frac{R_F}{R_G}$, there are two possible circuit solutions. First, when V_{IN} is a negative voltage, V_{OUT} must be a negative voltage. The circuit can not achieve a negative output voltage with a positive supply, so the output saturates at the lower power supply rail. Second, when V_{IN} is a positive voltage, the output spans the normal range as shown by equation 11.

$$V_{IN} \leq 0, \qquad V_{OUT} = 0 \qquad\qquad (65)$$

$$V_{IN} \geq 0, \qquad V_{OUT} = V_{IN} \qquad\qquad (66)$$

The noninverting op amp circuit is shown in Figure 8 with $V_{CC} = 5$ V, $R_G = R_F = 100$ K, $R_L = 10$ K, and $V_{REF} = 0$. The transfer curve for this circuit is shown in Figure 9; a TLV247X serves as the op amp.
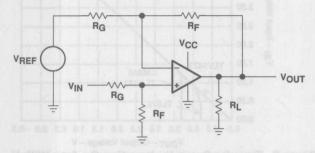
Figure 8. Noninverting Op Amp
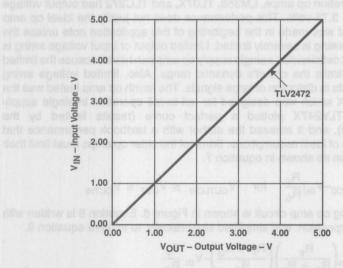
Figure 9. Transfer Curve for Noninverting Op Amp

There are many possible variations of inverting and noninverting circuits. At this point many designers analyze these variations hoping to stumble upon the one that solves the circuit problem. Rather than analyze each circuit, it is better to learn how to employ simultaneous equations to render specified data into equation form. When the form of the desired equation is known, a circuit that fits the equation is chosen to solve the problem. The resulting equation must be a straight line, thus there are only four solutions each of which is given in this application note.

Simultaneous Equations

Taking an orderly path to developing a circuit that works the first time starts here; follow these steps until the equation of the op amp is determined. Use specifications and simultaneous equations to determine what form the op amp equation must have. Go to the section that illustrates that equation form (called a case), solve the equation to determine the resistor values, and you have a working solution.

A linear op amp transfer function is limited to the equation of a straight line.

$$y = \pm\, mx \pm b \tag{67}$$

The equation of a straight line has four possible solutions depending upon the sign of m, the slope, and b, the intercept; thus simultaneous equations yield solutions in four forms. Four circuits must be developed; one for each form of the equation of a straight line. The four equations, cases, or forms of a straight line are given in equations 13 through 16, where electronic terminology has been substituted for math terminology.

$$V_{OUT} = mV_{IN} + b \tag{68}$$

$$V_{OUT} = mV_{IN} - b \tag{69}$$

$$V_{OUT} = -\,mV_{IN} + b \tag{70}$$

$$V_{OUT} = -\,mV_{IN} - b \tag{71}$$

Given a set of two data points for V_{OUT} and V_{IN}, simultaneous equations are solved to determine m and b for the equation that satisfies the given data. The sign of m and b determines the type of circuit required to implement the solution. The given data is derived from the specifications; i. e., a sensor output signal ranging from 0.1 volts to 0.2 volts must be interfaced into an analog-to-digital converter which has an input voltage range of 1volt to 4 volts. These data points ($V_{OUT} = 1$ V @ $V_{IN} = 0.1$ V, $V_{OUT} = 4$ V @ $V_{IN} = 0.2$ V) are inserted into equation 13, as shown in equations 17 and 18, to obtain m and b for the specifications.

$$1 = m(0.1) + b \tag{72}$$

$$4 = m(0.2) + b \tag{73}$$

Multiply equation 17 by 2 and subtract it from equation 18.

$$2 = m(0.2) + 2b \tag{74}$$

$$b = -2 \tag{75}$$

After algebraic manipulation of equation 17, substitute equation 20 into equation 17 to obtain equation 21.

$$m = \frac{2 + 1}{0.1} = 30 \tag{76}$$

Now m and b are substituted back into equation 13 yielding equation 22.

$$V_{OUT} = 30V_{IN} - 2 \tag{77}$$

Notice, although equation 13 was the starting point, the form of equation 22 is identical to the format of equation 14. The specifications or given data determine the sign of m and b, and starting with equation 13, the final equation form is discovered after m and b are calculated. The next step is to develop a circuit that has an m = 30 and b = −2 to complete the problem solution. Circuits were developed for equations 13 through 16, and they are given under the headings Case 1 through Case 4 respectively.

Case1: $V_{OUT} = mV_{IN}+b$

The circuit configuration which yields a solution for Case 1 is shown in Figure 10. The figure includes two 0.01 µF capacitors. These capacitors are called decoupling capacitors, and they are included to reduce noise and provide increased noise immunity. Sometimes two 0.01 µF capacitors serve this purpose, sometimes more extensive filtering is needed, sometimes one capacitor serves this purpose, but when V_{CC} is used as a reference, special attention must be paid to the regulation and noise content of V_{CC}.
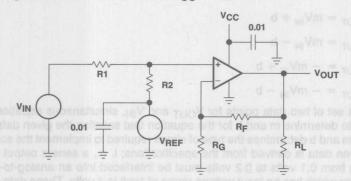
Figure 10. Schematic for Case1: $V_{OUT} = mV_{IN} + b$

The circuit equation is written using the voltage divider rule and superposition.

$$V_{OUT} = V_{IN}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{78}$$

The equation of a straight line (case 1) is repeated below so comparisons can be made between it and equation 23.

$$V_{OUT} = mV_{IN} + b \tag{79}$$

Term-by-term comparisons yield equations 25 and 26.

$$m = \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{80}$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{81}$$

Example; the circuit specifications are $V_{OUT} = 1$ V at $V_{IN} = 0.01$ V, $V_{OUT} = 4.5$ V at $V_{IN} = 1$ V, $R_L = 10$ K, five per cent resistor tolerances, and $V_{CC} = 5$ V. No reference voltage is available, thus V_{CC} is used for the reference input, and $V_{REF} = 5$ V. A reference voltage source is left out of the design as a space and cost savings measure, and it sacrifices noise, accuracy, and stability performance. Cost is an important specification, and the V_{CC} supply must be specified well enough to do the job. Each step in the subsequent design procedure is included in this analysis to ease learning and increase boredom. Many steps are skipped when subsequent cases are analyzed.

The data is substituted into simultaneous equations.

$$1 = m(0.01) + b \tag{82}$$

$$4.5 = m(1.0) + b \tag{83}$$

Equation 27 is multiplied by 100 (equation 29) and equation 28 is subtracted from equation 29 to obtain equation 30.

$$100 = m(1.0) + 100b \tag{84}$$

$$b = \frac{95.5}{99} = 0.9646 \tag{85}$$

The slope of the transfer function, m, is obtained by substituting b into equation 27.

$$m = \frac{1-b}{0.01} = \frac{1-0.9646}{0.01} = 3.535 \tag{86}$$

Now that b and m are calculated, the resistor values can be calculated. Equations 25 and 26 are solved for the quantity $(R_F + R_G)/R_G$, and then they are set equal in equation 32 thus yielding equation 33.

$$\frac{R_F + R_G}{R_G} = m\left(\frac{R_1 + R_2}{R_2}\right) = \frac{b}{V_{CC}}\left(\frac{R_1 + R_2}{R_1}\right) \tag{87}$$

$$R_2 = \frac{3.535}{\frac{0.9646}{5}} R_1 = 18.316 R_1 \tag{88}$$

Five per cent tolerance resistors are specified for this design, so we choose $R_1 = 10$K, and that sets the value of $R_2 = 183.16$ K. The closest 5% resistor value to 183.16 K is 180 K; therefore, select $R_1 = 10$ K and $R_2 = 180$ K. Being forced to yield to reality by choosing standard resistor values means that there is an error in the circuit transfer function because m and b are not exactly the same as calculated. The real world constantly forces compromises into circuit design, but the good circuit designer accepts the challenge and throws money or brains at it. Resistor values closer to the calculated values could be selected by using 1% or 0.5% resistors, but that selection increases cost and violates the design specification. The cost increase is hard to justify except in precision circuits. Using ten cent resistors with a ten cent op amp usually is false economy.

The left half of equation 32 is used to calculate R_F and R_G.

$$\frac{R_F + R_G}{R_G} = m\left(\frac{R_1 + R_2}{R_2}\right) = 3.535\left(\frac{180 + 10}{180}\right) = 3.73 \tag{89}$$

$$R_F = 2.73R_G \tag{90}$$

The resulting circuit equation is given below.

$$V_{OUT} = 3.5V_{IN} + 0.97 \tag{91}$$

The gain setting resistor, R_G, is selected as 10K, and 27 K, the closest 5% standard value is selected for the feedback resistor, R_F. Again, there is a slight error involved with standard resistor values. This circuit must have an output voltage swing from 1 to 4.5 volts. The older op amps can not be used in this circuit because they lack dynamic range, so the TLV247X family of op amps is selected. The data shown in Figure 7 confirms the op amp selection because there is little error. The circuit with the selected component values is shown in Figure 11. The circuit was built with the specified components, and the transfer curve is shown in Figure 12.
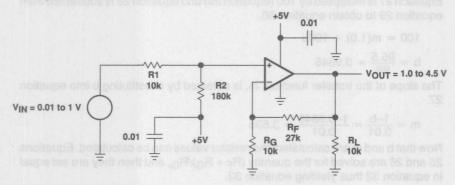
Figure 11. Case 1 Example Circuit
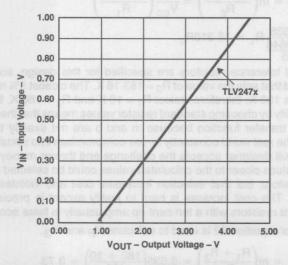
Figure 12. Case 1 Example Circuit Measured Transfer Curve

The transfer curve shown is a straight line, and that means that the circuit is linear. The V_{OUT} intercept is about 0.98 volts rather than 1 volt as specified, and this is excellent performance considering that the components were selected randomly from bins of resistors. Different sets of components would have slightly different slopes because of the resistor tolerances. The TLV247X has input bias currents and input offset voltages, but the effect of these errors is hard to measure on the scale of the output voltage. The output voltage measured 4.53 volts when the input voltage was 1 volt. Considering the low and high input voltage errors, it is safe to conclude that the resistor tolerances have skewed the gain slightly, but this is still excellent performance for 5% components. Often lab data similar to that shown here is more accurate than the 5% resistor tolerance, but do not fall into the trap of expecting this performance, because you will be disappointed if you do.

The resistors were selected in the K ohm range arbitrarily. The gain and offset specifications determine the resistor ratios, but supply current, frequency response, and op amp drive capability determine their absolute values. The resistor value selection in this design is high because modern op amps do not have input current offset problems, and they yield reasonable frequency response. If higher frequency response is demanded, the resistor values must decrease, and resistor value decreases reduce input current errors, while supply current increases. When the resistor values get low enough, it becomes hard for another circuit, or possibly the op amp, to drive the resistors.

Case 2: $V_{OUT} = mV_{IN} - b$

The circuit shown in figure 13 yields a solution for Case 2. The circuit equation is obtained by taking the Thevenin equivalent circuit looking into the junction of R_1 and R_2. After the R_1, R_2 circuit is replaced with the Thevenin equivalent circuit, the gain is calculated with the ideal gain equation (equation 37).
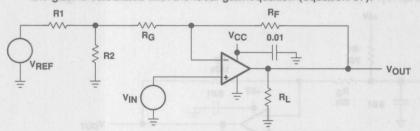
Figure 13. Schematic for Case 2; $V_{OUT} = mV_{IN} - b$

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G + R_1 \parallel R_2}{R_G + R_1 \parallel R_2}\right) - V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 \parallel R_2}\right) \quad (92)$$

Comparing terms in equations 37 and 14 enables the extraction of m and b.

$$m = \frac{R_F + R_G + R_1 \parallel R_2}{R_G + R_1 \parallel R_2} \quad (93)$$

$$|b| = V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1 + R_2}\right) \quad (94)$$

The specifications for an example design are: $V_{OUT} = 1.5V$ @ $V_{IN} = 0.2V$, $V_{OUT} = 4.5V$ @ $V_{IN} = 0.5V$, $V_{REF} = V_{CC} = 5V$, $R_L = 10K$, and 5% resistor tolerances. The simultaneous equations, 40 and 41, are written below.

$$1.5 = 0.2m + b \tag{95}$$

$$4.5 = 0.5m + b \tag{96}$$

From these equations we find that $b = -0.5$ and $m = 10$. Making the assumption that $R_1 || R_2 << R_G$ simplifies the calculations of the resistor values.

$$m = 10 = \frac{R_F + R_G}{R_G} \tag{97}$$

$$R_F = 9R_G \tag{98}$$

Let $R_G = 20K$, and then $R_F = 180K$.

$$b = V_{CC}\left(\frac{R_F}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) = 5\left(\frac{180}{20}\right)\left(\frac{R_2}{R_1 + R_2}\right) \tag{99}$$

$$R_1 = \frac{1 - 0.01111}{0.01111}R_2 = 89R_2 \tag{100}$$

Select $R_2 = 0.82K$ and R_1 equals 72.98 K. Since 72.98 K is not a standard 5% resistor value, R_1 is selected as 75 K. The difference between the selected and calculated value of R_1 has about a 3% effect on b, and this error shows up in the transfer function as an intercept rather than a slope error. The parallel resistance of R_1 and R_2 is approximately .82K and this is much less than R_G which is 20K, thus the earlier assumption that $R_G >> R1||R2$ is justified. R_2 could have been selected as a smaller value, but the smaller values yielded poor standard 5% values for R_1. The measured transfer curve for this circuit is shown in Figure 15.
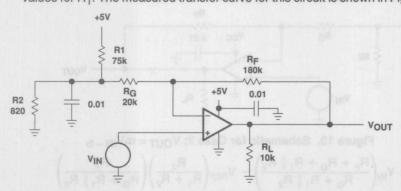
Figure 14. Case 2 Example Circuit
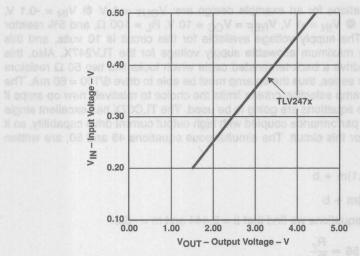
Figure 15. Case 2 Example Circuit Measured Transfer Curve

The TLV247X was used to build the test circuit because of its wide dynamic range. The transfer curve plots very close to the theoretical curve, and this results from a high performance op amp.

Case 3: $V_{OUT} = -mV_{IN} + b$

The circuit shown in Figure 16 yields the transfer function desired for Case 3.
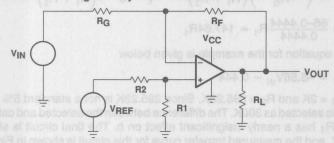
Figure 16. Schematic for Case 3; $V_{OUT} = -mV_{IN} + b$

The circuit equation is obtained with superposition.

$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \qquad 101)$$

Comparing terms between equations 45 and 15 enables the extraction of m and b.

$$|m| = \frac{R_F}{R_G} \qquad 102)$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \qquad 103)$$

The specifications for an example design are: $V_{OUT} = 1$ V @ $V_{IN} = -0.1$ V, $V_{OUT} = 6$ V @ $V_{IN} = -1$ V, $V_{REF} = V_{CC} = 10$ V, $R_L = 100$ Ω, and 5% resistor tolerances. The supply voltage available for this circuit is 10 volts, and this exceeds the maximum allowable supply voltage for the TLV247X. Also, this circuit must drive a back-terminated cable which looks like two 50 Ω resistors connected in series, thus the op amp must be able to drive 6/100 = 60 mA. The stringent op amp selection criteria limits the choice to relatively new op amps if ideal op amp equations are going to be used. The TLC07X has excellent single supply input performance coupled with high output current drive capability, so it is selected for this circuit. The simultaneous equations 49 and 50, are written below.

$$1 = (-0.1)m + b \qquad\qquad 104)$$

$$6 = (-1)m + b \qquad\qquad 105)$$

From these equations we find that b = 0.444 and m = –5.6.

$$|m| = 5.56 = \frac{R_F}{R_G} \qquad\qquad 106)$$

$$R_F = 5.56R_G \qquad\qquad 107)$$

Let $R_G = 10K$, and then $R_F = 56.6K$ which is not a standard 5% value, hence R_F is selected as 56K.

$$b = V_{CC}\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) = 10\left(\frac{56 + 10}{10}\right)\left(\frac{R_2}{R_1 + R_2}\right) \qquad\qquad 108)$$

$$R_2 = \frac{66-0.4444}{0.4444}R_1 = 147.64R_1 \qquad\qquad 109)$$

The final equation for the example is given below

$$V_{OUT} = -5.56V_{IN} - 0.444 \qquad\qquad 110)$$

Select $R_1 = 2K$ and $R_2 = 295.28K$. Since 295.28K is not a standard 5% resistor value R_1 is selected as 300K. The difference between the selected and calculated value of R_1 has a nearly insignificant effect on b. The final circuit is shown in Figure 17, and the measured transfer curve for this circuit is shown in Figure 18.
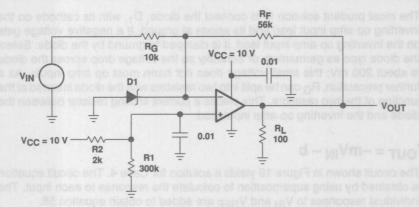
Figure 17. Case 3 Example Circuit
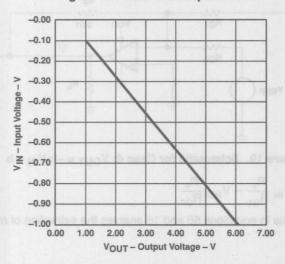
Figure 18. Case 3 Example Circuit Measured Transfer Curve

As long as the circuit works normally, there are no problems handling the negative voltage input to the circuit, because the inverting lead of the TLC07X is at a positive voltage. The positive op amp input lead is at a voltage of approximately 65 mV, and normal op amp operation keeps the inverting op amp input lead at the same voltage because of the assumption that the error voltage is zero. When V_{CC} is powered down while there is a negative voltage on the input circuit, most of the negative voltage appears on the inverting op amp input lead.

The most prudent solution is to connect the diode, D_1, with its cathode on the inverting op amp input lead and its anode at ground. If a negative voltage gets on the inverting op amp input lead, it is clamped to ground by the diode. Select the diode type as germanium or Schottky so the voltage drop across the diode is about 200 mV; this small voltage does not harm most op amp inputs. As a further precaution, R_G can be split into two resistors with the diode inserted at the junction of the two resistors. This places a current limiting resistor between the diode and the inverting op amp input lead.

Case 4: $V_{OUT} = -mV_{IN} - b$

The circuit shown in Figure 19 yields a solution for Case 4. The circuit equation is obtained by using superposition to calculate the response to each input. The individual responses to V_{IN} and V_{REF} are added to obtain equation 56.
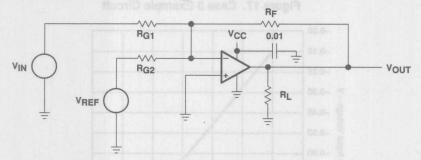
Figure 19. Schematic for Case 4; $V_{OUT} = -mV_{IN} - b$

$$V_{OUT} = -V_{IN} \frac{R_F}{R_{G1}} - V_{REF} \frac{R_F}{R_{G2}}$$ (111)

Comparing terms in equations 56 and 16 enables the extraction of m and b.

$$|m| = \frac{R_F}{R_{G1}}$$ (112)

$$|b| = V_{REF} \frac{R_F}{R_{G2}}$$ (113)

The specifications for an example design are: $V_{OUT} = 1$ V @ $V_{IN} = -0.1$ V, $V_{OUT} = 5$ V @ $V_{IN} = -0.3$ V, $V_{REF} = V_{CC} = 5$ V, $R_L = 10$ K, and 5% resistor tolerances. The simultaneous equations 59 and 60, are written below.

$$1 = (-0.1)m + b$$ (114)

$$5 = (-0.3)m + b$$ (115)

From these equations we find that b = -1 and m = -20. Setting the magnitude of m equal to equation 57 yields equation 61.

$$|m| = 20 = \frac{R_F}{R_{G1}}$$ (116)

$$R_F = 20R_{G1} \qquad \qquad \text{117)}$$

Let $R_{G1} = 1K$, and then $R_F = 20K$.

$$|b| = V_{CC}\left(\frac{R_F}{R_{G1}}\right) = 5\left(\frac{R_F}{R_{G2}}\right) = 1 \qquad \qquad \text{118)}$$

$$R_{G2} = \frac{R_F}{0.2} = \frac{20}{0.2} = 100 \ k \qquad \qquad \text{119)}$$

The final equation for this example is given in equation 63.

$$V_{OUT} = -20V_{IN} - 1 \qquad \qquad \text{120)}$$

The measured transfer curve for this circuit is shown in Figure 21.
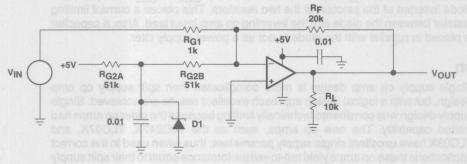
Figure 20. Case 4 Example Circuit
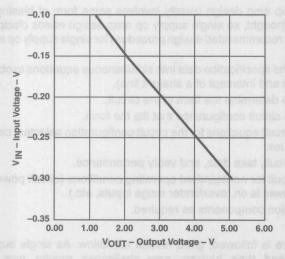
Figure 21. Case 4 Example Circuit Measured Transfer Curve

The TLV247X was used to build the test circuit because of its wide dynamic range. The transfer curve plots very close to the theoretical curve, and this results from using a high performance op amp.

As long as the circuit works normally there are no problems handling the negative voltage input to the circuit because the inverting lead of the TLV247X is at a positive voltage. The positive op amp input lead is grounded, and normal op amp operation keeps the inverting op amp input lead at ground because of the assumption that the error voltage is zero. When V_{CC} is powered down while there is a negative voltage on the input circuit, most of the negative voltage appears on the inverting op amp input lead.

The most prudent solution is to connect the diode, D_1, with its cathode on the inverting op amp input lead and its anode at ground. If a negative voltage gets on the inverting op amp input lead it is clamped to ground by the diode. Select the diode type as germanium or Schottky so the voltage drop across the diode is about 200 mV; this small voltage does not harm most op amp inputs. As a further precaution, R_{G2} is split into two resistors ($R_{G2A} = R_{G2B} = 51K$) with the diode inserted at the junction of the two resistors. This places a current limiting resistor between the diode and the inverting op amp input lead. Also, a capacitor is placed in parallel with the diode to act as a power supply filter.

Conclusion

Single supply op amp design is more complicated than split supply op amp design, but with a logical design approach excellent results are achieved. Single supply design was considered technically limiting because the older op amps had limited capability. The new op amps, such as the TLC247X, TLC07X, and TLC08X have excellent single supply parameters; thus when used in the correct applications these op amps yield rail-to-rail performance equal to their split supply counterparts.

Single supply op amp design usually involves some form of biasing, and this requires more thought, so single supply op amp design needs discipline and a procedure. The recommended design procedure for single supply op amp design is:

- Substitute the specification data into simultaneous equations to obtain m and b (the slope and intercept of a straight line).
- Let m and b determine the form of the circuit.
- Choose the circuit configuration that fits the form.
- Using the circuit equations for the circuit configuration selected, calculate the resistor values.
- Build the circuit, take data, and verify performance.
- Test the circuit for nonstandard operating conditions (circuit power off while interface power is on, over/under range inputs, etc.).
- Add protection components as required.
- Retest.

If this procedure is followed, good results will follow. As single supply circuit designers expand their horizon, new challenges require new solutions. Remember, the only equation a linear op amp can produce is the equation of a straight line. That equation only has four forms. The new challenges may consist of multiple inputs, common-mode voltage rejection, or something different, but the methods taught here can be expanded to meet these challenges.

Application of Rail-to-Rail Operational Amplifiers

Andreas Hahn   Mixed Signal Products

ABSTRACT

This application report assists design engineers to understand the functionality and benefits of rail-to-rail operational amplifiers. It shows simplified schematics, functions, and characteristics of the output and input stages. Typical application schematics for rail-to-rail operational amplifier are also discussed.

Contents

Introduction

Electrical applications increasingly use a single supply voltage of 5 V or less as portable electrical equipment becomes more popular. The supply voltage for portable systems can be as low as the voltage provided by one battery cell (1.5 V). Reduced supply voltage designs must use the complete power supply span to have a usable dynamic range. Operational amplifiers that use the complete span between negative and positive supply voltage for signal conditioning are generally known as rail-to-rail amplifiers. The usable span is an important value because it influences several parameters such as noise susceptibility, signal-to-noise ratio (SNR), and dynamic range. Signal sources are often connected to the positive or negative supply rail. Operational amplifiers need rail-to-rail input capability to match both signal sources with one device. This report explains the function and the use of rail-to-rail operational amplifiers.

Dynamic Range and SNR in Low Single Supply Systems

Reducing the operating supply voltage from a ±15-V split supply to a single 5-V supply significantly reduces the maximum available dynamic range. The dynamic range at the output is determined by the ratio of the largest output voltage to the smallest output voltage. An industry standard operational amplifier like the TLC271 is specified at 5-V single supply with 3.8 V$_{pp}$ for the maximum output swing. This means that the whole supply span can not be used for the output swing, resulting in a further reduction of the maximum available dynamic range and SNR. A rail-to-rail operational amplifier like the TLV24xx family can use the full span of the supply range for signal conditioning at the input and output.

Operational amplifier disturbance levels are independent of the supply voltage. This results in smaller spacing between usable and noise signals. If the operational amplifier is used with ac signals, by decoupling the signals from dc, then noise forms the determining disturbance signal. For a standard operational amplifier such as the TLC271C, the input noise voltage V$_n$ at a signal bandwidth of 1 MHz equals 68 μV†= 68 nV/$\sqrt{Hz}\cdot\sqrt{1\ MHz}$. With a 5-V single supply, the reduced output range allows a maximum signal level of 3.8 V$_{pp}$. This results in a unity gain configuration in a SNR of 95.4 dB=20 log(4 V/68 μV). In the same configuration, a rail-to-rail amplifier such as the TLV246xI with V$_n$=11 nV/$\sqrt{Hz}$ † and a maximum signal level of 5 V$_{pp}$ at the input and output provides a signal-to-noise ratio of 113 dB=20 log(5 V/11 μV) at BW=1 MHz.

In a precision system the operational amplifier must amplify the dc voltage level precisely. Errors in this area result from offset and gain problems. In a 5-V system with a constant common-mode voltage, the TLC271C has an input offset voltage V$_{IO}$ of 1.1 mV†. This alone limits the dynamic range to 71 dB=20 log(3800/1.1) in a unity gain configuration. The TLV245x, however, with V$_{IO}$ = 20 μV† and the rail-to-rail characteristic has a significantly higher dynamic range of 108 dB=20 log(5800/1.1) in the same circuitry.

†Typical values at 5 V single supply and 25°C.

When signal-to-noise ratio and dynamic range are critical design parameters, rail-to-rail characteristics of the operational amplifier must ensure that these parameters are met.

The Output Stage

If the output swing from a standard operational amplifier is not large enough to fit the system requirement (for example the analog-to-digital-converter input range), then a rail-to-rail operational amplifier must be used. Operational amplifiers with rail-to-rail output stages achieve the maximum output signal swing in systems with low single-supply voltages. They can generate an output signal up to the supply rails. A large output voltage swing results in increased dynamic range. For example, Figure 1 shows the output signal of a TLV2462 with a 5-V_{pp} input signal. The TLV2462 with a 5-V single supply operates as a voltage follower and drives a load of 1 kΩ. The low 1-kΩ load results in a voltage drop of several mV, which is not visible in the diagram.
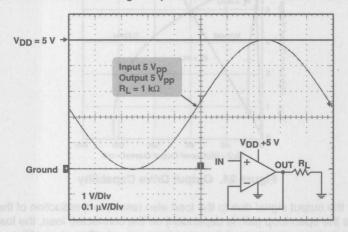
Figure 22. Rail-to-Rail Output Stage

Construction of a Rail-to-Rail Output Stage
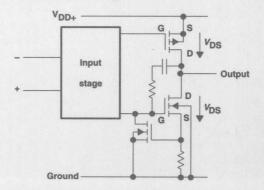
Figure 23. Output Stage of a TLC227x

The rail-to-rail characteristic is achieved by altering the output stage construction. Figure 2 shows the basic construction of a rail-to-rail CMOS output stage as used in the TLC227x. A complimentary MOS transistor pair, consisting of a self-locking P-channel and self-locking N-channel, forms the output. Both transistors operate as a common source circuit. A common source circuit functions like a common emitter circuit for bipolar transistors. Along with the current amplification, a voltage amplification also takes place. The voltage loss V_{DS} at the output stage transistors has a disadvantageous effect on the voltage gain. As the current increases through a MOS transistor the resistance between drain and source increases slightly. During high loading of the output, this resistance, together with the increased current, results in a higher voltage drop V_{DS}. The full output range of a rail-to-rail operational amplifier is therefore only useable with low load. Figure 3 shows this on the output level of the TLV243x and TLV246x.
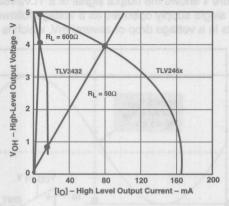
Figure 24. Output Drive Capability

Reduction of the output signal due to the load also results in a reduction of the open-loop gain A_{VD}. Because the open-loop gain is dependent on the connected load, the load should always be considered during comparison of the open-loop gain of different amplifiers. Figure 4 shows the influence of a resistive load on the amplification of a TLV246x.
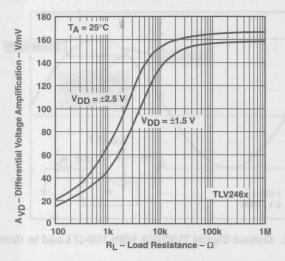
Figure 25. A/D Dependent on the Load for TLV246x

The Dependence of Output Signal Load

It is important to know which potential the load is connected to when talking about the behaviour of the output signal due to the load. In applications with a single supply, it is typical for the load to be connected to ground (0V). The requirement from a rail-to-rail output is the capability to supply a load with current. Figure 5 shows an example of this on a TLV2462. The TLV2462 functions as a unity gain amplifier and drives a 100-Ω load against the supply ground. Because of the 600-mV voltage drop across the output transistor caused by the current, the output can only drive the signal up to a maximum voltage level of 4.4 V. The minimum voltage level however, reaches the 0 V of the ground level. At an output voltage of 0 V, no current flows through the load, since both ends of the load are at the same potential. With no current, there is no voltage drop across the output transistor. With a load driven against ground, an output signal limitation due to the load current only occurs at high voltage levels.
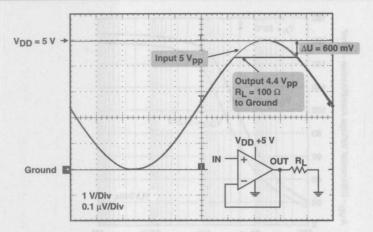
Figure 26. Output Signal TLV2462 With 100-Ω Load to Ground

A rail-to-rail output should not be limited to sourcing a load with current; it should also have the ability to sink a current. All rail-to-rail output stages of Texas Instruments have the capability of sourcing and sinking current. Figure 27 shows an example where the TLV2462 drives —as a unity amplifier— a load of 100 Ω against half the supply voltage $V_{DD}/2$. With a maximum input signal of 5 V_{pp} an output signal is produced as shown in Figure 6. In this case, at minimum and maximum voltage levels, the maximum current flows through the respective output transistor. The resulting voltage drop of 300 mV at the respective peak voltages restricts the output signal to 4.4 V_{pp}.
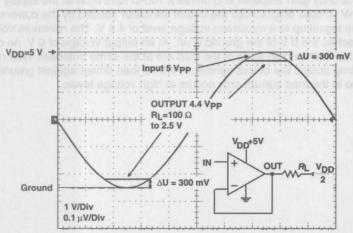
Figure 27. Output Signal TLV2462 With 100-Ω Load to $V_{DD}/2$

Slew Rate

Another important parameter, especially for ac application characteristics, is the slew rate of the output stage. The slew rate is a measure for the maximum possible voltage rise and fall speed, which is the ratio of the voltage change during a period of time. To reproduce a sine signal without distortion, use the following equation:

$$SR = 2\pi \, f_{max} \, V_p \qquad\qquad 121)$$

Equation 1 shows that if the output voltage is reduced by a lower supply voltage, the required slew rate decreases proportionally with the possible voltage level. This should be noted when comparing a CMOS rail-to-rail operational amplifier and a standard amplifier.

The standard amplifier with an output range of ±13 V requires a slew rate of 82 V/μs to accurately reproduce a 1-MHz sine wave signal with 26 V_{pp}. A rail-to-rail amplifier with a 3-V single supply needs only a slew rate of 9.4 V/μs to achieve a distortion free 1-MHz sine wave signal with 3 V_{pp}. The slew rate also depends on the load and decreases with increasing load.

Summary of Output Stage

Rail-to-rail output quality is only comparable with another under identical load. Without a load on the output, it is possible for every rail-to-rail operational amplifier to bring the output signal up to the supply rail. A rail-to-rail output should be capable of both sourcing and sinking current in order to also drive loads not connected to ground. Operational amplifiers supplied with low supply voltages can only provide low signal amplitudes, which require a lower slew rate.

The Input Stage

In some applications an operational amplifier requires a rail-to-rail input in addition to the rail-to-rail output. The signal at the input pins must be in the input common-mode voltage range V_{ICR} to ensure the functionality of the amplifier. A rail-to-rail input stage offers a V_{ICR} that minimally includes the whole supply span. The V_{ICR} of the TLV246x extends beyond the supply rails by 200 mV for maximum dynamic range in low-voltage systems. A rail-to-rail input has advantages and disadvantages; it is not required in every application, but only in applications where the input signal is outside a standard common-mode range. Figure 7 shows a typical operational amplifier configured as an inverting amplifier. The relationship of the resistances R_F and R_G determine the gain in the circuit. R_C compensates offset errors from the input bias current.

$$V_{OUT} = -\frac{R_F}{R_G} V_{IN} + \frac{R_F}{R_G} V_{ref} + V_{ref}$$

Figure 28. Inverting Amplifier

The noninverting input is connected to a fixed voltage level V_{ref}. The common-mode input voltage is maintained at a constant value, because the inverting input, via the feedback, takes the same reference potential as the noninverting input. In systems with a double supply, this is typically the circuit ground. In most cases it is half the supply voltage for single supply systems. The V_{ICR} of a standard operational amplifier in most cases contains this common-mode voltage level, mentioned above. If the reference level V_{ref} lies within this standard V_{ICR}, a circuit like that shown in Figure 7 does not necessarily require a rail-to-rail input stage.

The circuit shown in Figure 8 behaves differently. The inverting input here also follows the noninverting input via the feedback. In this case no fixed voltage level lies at the noninverting input, but the signal itself does. At high gains, the input signal is small and lies within the V_{ICR} of a standard operational amplifier. If the resistance R_G is removed, a unity gain amplifier, also called an impedance converter or voltage follower, is formed. This circuit produces a gain of 1 so that the input level is equal to the output level. If the entire output range of the rail-to-rail operational amplifier is used for signal conditioning, then a rail-to-rail input stage is also required. Impedance converters and high-side sensing applications are the main activity areas for operational amplifiers with rail-to-rail input and output.
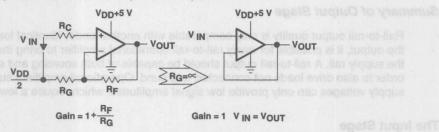
Figure 29. Change From Noninverting Amplifier to Buffer

Construction of a Standard Input Stage

On a standard operational amplifier using bipolar technology, the input differential amplifier, as shown in Figure 9, consists ideally of equal transistors. To achieve ground potential in the common-mode range, PNP transistors are primarily used here. Likewise in the MOS technology, P-channel transistors are used. There is a voltage drop of around 0.7 V across the PNP transistor and around 0.3 V across the bias current source. This results in a limited common-mode range, which always lies at least 1 V below the positive supply voltage. In the other direction, the V_{ICR} extends up to the negative supply voltage or slightly beyond. To enable use of the full supply voltage range, the construction of the standard differential amplifier has to be modified.
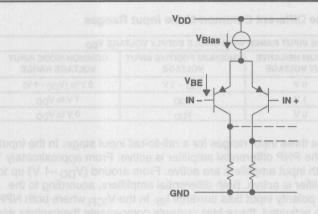
Figure 30. Differential Amplifier

Construction of a Rail-to-Rail Input Stage
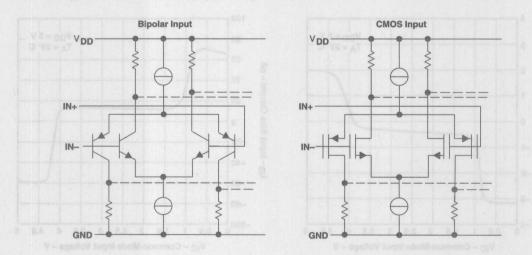
Figure 31. Rail-to-Rail Input Stage

There are various methods of constructing these types of input stages. Figure 31 shows the general construction of a rail-to-rail input stage using two different techniques. The bipolar input stage is used in the TLV245x and TLV246x. The input stage of the TLV247x series is designed in CMOS technology. The bipolar input stage in Figure 10 shows clearly that two differential amplifiers are being driven simultaneously. The differential amplifier with PNP transistors, mentioned before, works up to a maximum common-mode level of 1 V below the supply voltage. The differential amplifier working with NPN transistors requires a common-mode level of at least 1 V.

Texas Instruments

Table 2. The Different Common-Mode Input Ranges

	COMMON-MODE INPUT RANGE WITH SINGLE SUPPLY VOLTAGE V_{DD}		
DIFFERENCE AMPLIFIER TYPE	MAXIMUM NEGATIVE INPUT VOLTAGE	MAXIMUM POSITIVE INPUT VOLTAGE	COMMON-MODE INPUT VOLTAGE RANGE
PNP	0 V	$V_{DD} - 1$ V	0 V to $(V_{DD} - 1$ V$)$
NPN	1 V	V_{DD}	1 V to V_{DD}
PNP+NPN	0 V	V_{DD}	0 V to V_{DD}

As shown in Table 2, there are three input ranges for a rail-to-rail input stage. In the input range from 0 V to around 1 V, only the PNP differential amplifier is active. From approximately 1 V to approximately ($V_{DD} - 1$ V) both input amplifiers are active. From around ($V_{DD} - 1$ V) up to V_{DD} only the NPN differential amplifier is active. Both differential amplifiers, according to the transistor type, have different polarity input bias currents I_{IB}. In the V_{ICR} where both NPN and PNP differential amplifiers are activated, these bias currents compensate themselves and form a bias current around 1000 times smaller than a standard bipolar input stage. The input offset voltage V_{IO} also changes in each range, which depends on the activated differential amplifier. Figure 11 and Figure 12 show these two values for the TLV245x series. This characteristic has the benefit that in the range from around 1 V to ($V_{DD} - 1$ V) the input stage has lower input bias in comparison with values for a standard bipolar input stage typical of this technology.
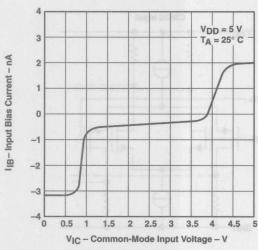
Figure 32. Input Bias Current
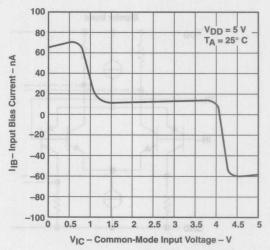
Figure 33. Input Offset Voltage

The different bias currents and offset voltages in Figure 11 and Figure 12 result in a different output error in each range. If the whole input range is used, distortion is generated at the transitions of the individual ranges. By connecting a series resistance R_C as shown in Figure 7 and Figure 8, it is possible to reduce the errors at the transitions caused by the bias currents. The required resistance is as follows:

$$R_C = \frac{R_G \times R_F}{R_G + R_F}$$

122)

The bias current at the resistors now causes an equal voltage drop at both inputs. To minimize a voltage drop caused by the bias current, all resistance values must be kept as small as possible for the application. Typical values for R_C lie below 10 kΩ. This significantly reduces the transient distortions.
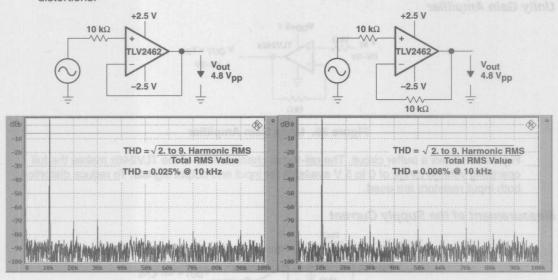
Figure 34. Minimizing the Transient Distortions (THD)

To emphasize the function of the compensation resistor, large resistance values of 10 kΩ have been deliberately selected for the circuit shown in Figure 13. Both noninverting amplifiers are set to a gain of 1. The left amplifier operates without a resistance in the feedback circuit. For compensation, both inputs on the right amplifier are connected with an equal resistance. This balances the voltage drops on both inputs, which are caused by the input currents. This reduces the total harmonic distortion (THD) from 0.025% to 0.008%.

Summary of the Input Stage

This section shows that a rail-to-rail input is not required in every application. In many cases, a standard input range, such as that of a TLC450x, is sufficient. The main advantage of a rail-to-rail input is the higher common-mode input range. It is possible to drive the amplifier in the entire common-mode input range from 0 V up to V_{DD} and above both rails. A disadvantage is the additional distortion caused by the transitions in the common-mode input range. The rail-to-rail input stage behaves like a normal standard input stage if the common-mode voltage is fixed or fits in one field of the common-mode input range.

Circuits Which Use the Rail-to-Rail Characteristics

The following circuits use the rail-to-rail benefits.

Unity Gain Amplifier
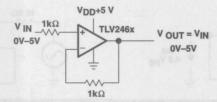
Figure 35. Unity Gain Amplifier

Figure 14 shows a buffer circuit. The rail-to-rail characteristic of the TLV246x makes the full operating voltage range of 0 to 5 V available for input and output signals. To reduce distortion both input resistors are used.

Measurement of the Supply Current
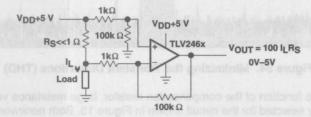
Figure 36. Unity Gain Amplifier

The rail-to-rail input of the TLV246x in the circuit shown in Figure 36 allows measurement of the load current in a 5-V system. The load current through R_L is measured by applying the voltage drop across the shunt resistor R_S to the differential input. This input voltage is amplified 100 times. The rail-to-rail output allows output voltages, which extend up to the supply voltage, to be generated. The output voltage is proportional to the load current. Selecting an appropriate shunt resistor R_S for the circuit can set the maximum load current. R_S is therefore calculated as follows:

$$R_S = \frac{0.05 \text{ V}}{I_{Lmax}}$$
123)

Differential Amplifier With Rail-to-Rail Output

$$V_{OUT} = V_{IN}\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + V_{REF}$$

$$= 0\,V - 5\,V$$
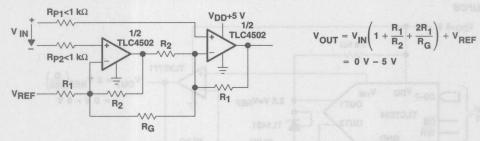
Figure 37. Instrument Amplifier With Two Operational Amplifiers

The TLC4502, with a typical common-mode rejection of 100 dB and a low temperature drift of 1 µV/°K, has outstanding characteristics for constructing an instrument amplifier, as shown in Figure 16. A high input impedance for the differential signal is achieved by using two operational amplifiers. The two resistors R_{P1} and R_{P2} provide protection against excessive input currents. The resistors R_1 and R_2 must have a tolerance of ≤0.1% to achieve high common-mode rejection. The resistor R_G adjusts the gain of the entire differential amplifier. The rail-to-rail output signal is calculated using the following equation:

$$U_{OUT} = U_{IN}\left(1 + \frac{R_1}{R_2} + \frac{2R_1}{R_G}\right) + U_{REF} \tag{124}$$

5-V_{PP} Square Wave Oscillator Up to 600 kHz
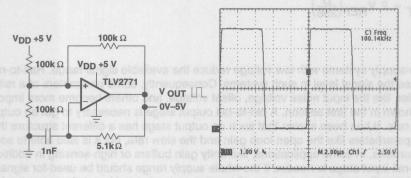
Figure 38. 100-kHz Square Wave Oscillator With 5 V_{PP}

Figure 17 shows a 5-V square wave generator using the rail-to-rail amplifier TLV277x. The amplifier offers a rail-to-rail output and a slew rate of 10.5 V/µs. In this circuit, the TLV277x can deliver at the output a 5-Vpp square wave up to 600 kHz. The frequency is independent of the operating voltage. The output frequency depends on the value of the resistors and the capacitor.

Digital-to-Analog Converter With a Rail-to-Rail Output as an Adjustable Reference Voltage Source
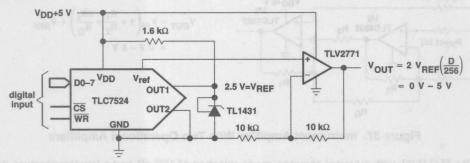
Figure 39. 5-V Digital-to-Analog Converter With 0 to 5-V Output

The combination of the digital-to-analog converter TLC7524 and the rail-to-rail operational amplifier TLV2771 shown in Figure 39, forms an 8-bit digital-to-analog converter powered by a single-voltage supply of 5 V. The TLV2771 can drive a 600-Ω load, which allows the converter to be used as a digitally adjustable reference voltage source for loads $\geq$ 600 Ω.

The TLC7524 supplies a digitally-adjustable output voltage of V_{REF} = D/256. The reference voltage V_{REF} is generated with the TL1431 with an accuracy of 0.4 %. The TLV2771 works as an impedance converter with a gain of 2. The total output voltage of the circuit is calculated as follows:

$$V_{OUT} = 2\ V_{REF}\left(\frac{D}{256}\right) \tag{125}$$

Summary

Single-supply systems with low voltage reduce the available signal range. Rail-to-rail amplifiers increase the signal level in such systems. Consequently, some parameters of a rail-to-rail amplifier, like the input noise voltage, offset voltage, and others become more important, which was shown in the first section. A rail-to-rail output stage is necessary to get an output swing up to the rails. It has been shown that such an output stage has a different structure that influences some parameters like the open loop gain and the slew rate, but it is also able to source and sink high currents. In some applications, like unity gain buffers or high-sensing in addition, a rail-to-rail input stage is needed if the whole supply range should be used for signal conditioning. It has been illustrated how a rail-to-rail input stage works and how it improves the input common mode range. Drawbacks have also been shown. Finally, the report shows some typical applications for rail-to-rail amplifiers.

References

12. Linear Design Seminar 99, Texas Instruments Incorporated, 1999

13. TL1431 Data sheet SLVS062C , Texas Instruments Incorporated, July 1998

14. TLC450x Data sheet SLOS221, Texas Instruments Incorporated, May 1998

15. TLC7424 Data sheet SLAS061C, Texas Instruments Incorporated, Nov. 1998

16. TLV245x Data sheet SLOS218A , Texas Instruments Incorporated, April 1999

17. TLV246x Data sheet SLOS220A , Texas Instruments Incorporated, August 1998

18. TLV247x Data sheet SLOS232 , Texas Instruments Incorporated, May 1999

19. TLV277x Data sheet SLOS209A ,Texas Instruments Incorporated, July 1998

20. Rail-to-Rail Verstärker in Niederspannungssystemen, Artikel "Extrem Sparsam", Elektronik Praxis Nr.7 April 1999 (Rail-to-rail amplifiers in low-voltage systems, Article "extremely economical", Practical Electronics No. 7, April 1999)

21. Halbleiter Schaltungstechnik, Tietze & Schenk, Springer Verlag 1993 (Semiconductor circuit technology, publishers: Tietze & Schenk, Springer Verlag 1993)

22. Professionelle Schaltungstechnik mit Operationsverstärker, Horst Wupper, Franzis-Verlag GmbH, 1994 (Professional circuit technology with operation amplifiers, publishers: Horst Wupper, Franzis-Verlag GmbH, 1994)

References

12. Linear Design Seminar 93, Texas Instruments Incorporated, 1993

13. TL1431 Data sheet SLVS082C, Texas Instruments Incorporated, July 1998

14. TLC4501x Data sheet SLOS221, Texas Instruments Incorporated, May 1998

15. TLC7424 Data sheet SLAS061C, Texas Instruments Incorporated, Nov. 1998

16. TLV245x Data sheet SLOS218A, Texas Instruments Incorporated, April 1999

17. TLV246x Data sheet SLOS232A, Texas Instruments Incorporated, August 1998

18. TLV247x Data sheet SLOS232, Texas Instruments Incorporated, May 1999

19. TLV277x Data sheet SLOS209A, Texas Instruments Incorporated, July 1998

20. Rail-to-Rail Verstärker in Niederspannungssystemen, Artikel "Extrem Sparsam", Elektronik Praxis Nr.7 April 1999 (Rail-to-rail amplifiers in low-voltage systems, Article "extremely economical," Practical Electronics No. 7, April 1999)

21. Halbleiter Schaltungstechnik, Tietze & Schenk, Springer Verlag 1993 (Semiconductor circuit technology, publishers; Tietze & Schenk, Springer Verlag 1993)

22. Professionelle Schaltungstechnik mit Operationsverstärkern, Horst Wupper, Franzis-Verlag GmbH, 1994 (Professional circuit technology with operation amplifiers, publishers: Horst Wupper, Franzis-Verlag GmbH, 1994)

![Texas Instruments logo] **TEXAS INSTRUMENTS**

Understanding Basic Analog - Circuit Equations

Application Report

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Understanding Basic Analog—Circuit Equations

By Ron Mancini

ABSTRACT

This application report provides a basic understanding of analog circuit equations. Only sufficient math and physics are presented in this application report to enable understanding the concepts.

Introduction

Although this application note tries to minimize math, some algebra is germane to the understanding of analog electronics. Math and physics are presented in this application note in the manner in which they are used later, so no practice exercises are given. For example, after the voltage divider rule is explained, it is used several times in the development of other concepts, and this usage constitutes the practice. This application note builds on each concept after it has been explained, thus, if you want to get familiar with the concepts, read it from beginning to end.

Circuits are a mix of passive and active components. The components are arranged in a manner that enables them to perform some desired function. The resulting arrangement of components is called a circuit or sometime a circuit configuration. The art portion of analog design is designing the circuit configuration. There are many published circuit configurations for almost any circuit task, thus all circuit designers need not be artists.

When the design has progressed to the point that a circuit exists, equations must be written to predict and analyze circuit performance. Textbooks are filled with rigorous methods for equation writing, and this application note does not supplant those textbooks. But, a few equations are used so often that they should be memorized, and these equations are considered here.

There are almost as many ways to analyze a circuit as there are electronic engineers, and if the equations are written correctly, all methods yield the same answer. There are some simple ways to analyze the circuit without completing unnecessary calculations, and these methods are illustrated here.

Laws of Physics

Ohm's law is stated as $V=IR$, and it is fundamental to all electronics. Ohm's law can be applied to a single component, to any group of components, or to a complete circuit. When the current flowing through any portion of a circuit is known, the voltage dropped across that portion of the circuit is obtained by multiplying the current times the resistance.

Figure 40. Ohm's Law Applied to the Total Circuit

$$V = IR$$ 126)

In Figure 1, Ohm's law is applied to the total circuit. The current, (I) flows through the total resistance (R), and the voltage (V) is dropped across R. In Figure 2, Ohm's law is applied to a single component. The current (I_R) flows through the resistor (R) and the voltage (V_R) is dropped across R. Notice, the same formula is used to calculate the voltage drop regardless of what portion of the circuit the calculation is made on.
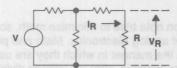
Figure 41. Ohm's Law Applied to a Component

Kirchoff's voltage law states that the sum of the voltage drops in a series circuit equals the sum of the voltage sources. Otherwise, the source (or sources) voltage must be dropped across the passive components. When taking sums keep in mind that the sum is an algebraic quantity.
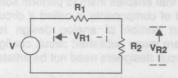
Figure 42. Kirchoff's Voltage Law

$$\sum V_{SOURCES} = \sum V_{DROPS}$$ 127)

$$V = V_{R1} + V_{R2}$$ 128)

Kirchoff's current law states; the sum of the currents entering a junction equals the sum of the currents leaving a junction. It makes no difference if a current flows from a current source, through a component, or through a wire, because all currents are equal. Kirchoff's law is illustrated in Figure 4.
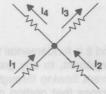
Figure 43. Kirchoff's Current Law

$$\sum I_{IN} = \sum I_{OUT} \qquad \text{129)}$$

$$I_1 + I_2 = I_3 + I_4 \qquad \text{130)}$$

Voltage Divider Rule

When the output of a circuit is not loaded, the voltage divider rule can be used to calculate the circuit's output voltage. Assume that the same current flows through all circuit elements. Equation 6 is written using Ohm's law as $V = I (R_1 + R_2)$. Equation 7 is written as Ohm's law across the output resistor.
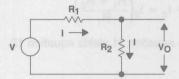
Figure 44. Voltage Divider Rule

$$I = \frac{V}{R_1 + R_2} \qquad \text{131)}$$

$$V_D = IR_2 \qquad \text{132)}$$

Substituting equation 6 into equation 7, and using algebraic manipulation yields equation 8.

$$V_D = V \frac{R_2}{R_1 + R_2} \qquad \text{133)}$$

A simple way to remember the voltage divider rule is that the output resistor is divided by the total circuit resistance. This fraction is then multiplied by the input voltage to obtain the output voltage. Remember that the voltage divider rule always assumes that the output resistor is not loaded; the equation is not valid when the output resistor is loaded by parallel component. Fortunately, most circuits following a voltage divider are input circuits, and input circuits are usually high resistance. When a fixed load is in parallel with the output resistor, the equivalent parallel value comprised of the output resistor and loading resistor can be used in the voltage divider calculations with no error. Many people ignore the load resistor if it is ten times greater than the output resistor value, but this calculation can lead to a 10% error.

Current Divider Rule

When the output of a circuit is not loaded, the current divider rule can be used to calculate the current flow in the output branch circuit (R_2). The currents I_1 and I_2 in Figure 6 are assumed to be flowing in the branch circuits. Equation 9 is written with the aid of Kirchoff's current law. The circuit voltage is written in equation 10 with the aid of Ohm's law. Combining equations 9 and 10 yields equation 11.
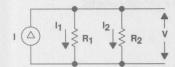
Figure 45. Current Divider Rule

$$I = I_1 + I_2 \tag{134}$$

$$V = I_1 R_1 = I_2 R_2 \tag{135}$$

$$I = I_1 + I_2 = I_2\frac{R_2}{R_1} + I_2 = I_2\left(\frac{R_1 + R_2}{R_1}\right) \tag{136}$$

Rearranging the terms in equation 11 yields equation 12.

$$I_2 = I\left(\frac{R_1}{R_1 + R_2}\right) \tag{137}$$

The total circuit current divides into two parts, and the resistance (R_1) divided by the total resistance determines how much current flows through R_2. An easy method of remembering the current divider rule is to remember the voltage divider rule. Then modify the voltage divider rule such that the opposite resistor is divided by the total resistance, and the fraction is multiplied by the input current to get the branch current.

Thevenin's Theorem

There are times when it is advantageous to isolate a part of the circuit, and analyze just the isolated part of the circuit. Rather than write loop or node equations for the complete circuit, and solving them simultaneously, Thevenin's theorem enables us to isolate the part of the circuit we are interested in. We then replace the remaining circuit with a simple series equivalent circuit, thus Thevenin's theorem simplifies the analysis.

There are two theorems that do the similar functions, and the second theorem is called Norton's theorem. Thevenin's theorem is used when the input driver is a voltage source, and Norton's theorem is used when the input drive is a current source. Norton's theorem is rarely used, so its explanation is left for the reader to dig out of a textbook if it is ever required.
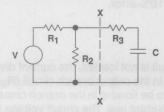
Figure 46. Original Circuit

The rules for Thevenin's theorem start with the component or part of the circuit being replaced. Referring to Figure 7, look into the terminals (point XX in the figure) of the circuit being replaced. Calculate the no load voltage (V_{TH}) as seen from these terminals (use the voltage divider rule). Look into the terminals of the circuit being replaced, short independent voltage sources, and calculate the impedance between these terminals. The final step is to substitute the Thevenin equivalent circuit for the part you wanted to replace.

Figure 47. Thevenin's Equivalent Circuit for Figure 7

The Thevenin equivalent circuit is a simple series circuit, thus further calculations are simplified. The simplification of circuit calculations is often sufficient reason to use Thevenin's theorem because it eliminates the need for solving several simultaneous equations. The detailed information about what happens in the circuit that was replaced is not available when using Thevenin's theorem, but that is no consequence because you had no interest in it.

As an example of Thevenin's theorem, let's calculate the output voltage (V_O) shown in Figure 9A. The first step is to stand on the terminals X–Y with your back to the output circuit, and calculate the open circuit voltage seen. This is a perfect opportunity to use the voltage divider rule to obtain equation 13.

(a) The Original Circuit

(b) The Thevenin Equivalent Circuit
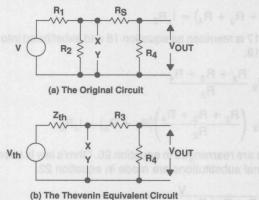
Figure 48. Example of Thevenin's Equivalent Circuit

$$V_{TH} = V \frac{R_2}{R_1 + R} \qquad (138)$$

Still standing on the terminals X-Y, step two is to calculate the impedance seen looking into these terminals (short the voltage sources). The Thevenin impedance is the parallel impedance of R_1 and R_2 as calculated in equation 14. Now get off the terminals X-Y before you damage them with your big feet. Step three replaces the circuit to the left of X-Y with the Thevenin equivalent circuit V_{TH} and R_{TH}.

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$
(139)

The final step is to calculate the output voltage. Notice the voltage divider rule is used again. Equation 15 describes the output voltage, and it comes out naturally in the form of a series of voltage dividers, which makes sense. That's another advantage of the voltage divider rule; the answers normally come out in a recognizable form rather than a jumble of coefficients and parameters.

$$V_{OUT} = V_{TH} \frac{R_4}{R_{TH} + R_3 + R_4} = V\left(\frac{R_2}{R_1 + R_2}\right) \frac{R_4}{\frac{R_1 R_2}{R_1 + R_2} + R_3 + R_4}$$
(140)

The circuit analysis is done the hard way in Figure 10, so you can see the advantage of using Thevenin's Theorem. Two loop currents, I_1 and I_2, are assigned to the circuit. Then the loop equations 16 and 17 are written.
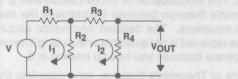
Figure 49. Analysis Done the Hard Way

$$V = I_1(R_1 + R_2) - I_2 R_2$$
141)

$$I_2(R_2 + R_3 + R_4) = I_1 R_2$$
142)

Equation 17 is rewritten as equation 18 and substituted into equation 16 to obtain equation 19.

$$I_1 = I_2 \frac{R_2 + R_3 + R_4}{R_2}$$
(143)

$$V = I_2\left(\frac{R_2 + R_3 + R_4}{R_2}\right)(R_1 + R_2) - I_2 R_2$$
(144)

The terms are rearranged in equation 20. Ohm's law is used to write equation 21, and the final substitutions are made in equation 22.

$$I_2 = \frac{V}{\frac{R_2 + R_3 + R_4}{R_2}(R_1 + R_2) - R_2}$$
(145)

$$V_{OUT} = I_2 R_4$$
(146)

$$V_{OUT} = V \frac{R_4}{\frac{(R_2 + R_3 + R_4)(R_1 + R_2)}{R_2} - R_2}$$
(147)

This is a lot of extra work for no gain. Also, the answer is not in a usable form because the voltage dividers are not recognizable, thus more algebra is required to get the answer into usable form.

Superposition

Superposition is a theorem that can be applied to any linear circuit. Essentially, when there are independent sources, the voltages and currents resulting from each source can be calculated separately, and the results are added algebraically. This simplifies the calculations because it prevents writing a series of loop or node equations.
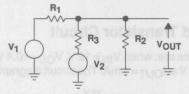
Figure 50. Superposition Example

When V_1 is grounded, V_2 forms a voltage divider with R_3 and the parallel combination of R_2 and R_1. The output voltage for this circuit (V_{OUT1}) is calculated with the aid of the voltage divider equation. The circuit is shown in Figure 12. The voltage divider theorem yields the answer quickly.
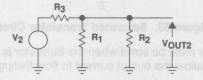
Figure 51. When V_1 is Grounded

$$V_{OUT2} = V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2}$$
(148)

Likewise, when V_2 is grounded, V_1 forms a voltage divider with R_1 and the parallel combination of R_3 and R_2, and the voltage divider theorem is applied again to calculate V_{OUT1}.
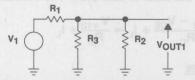
Figure 52. When V_2 is Grounded

$$V_{OUT1} = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3}$$
(149)

After the calculations for each source are made the components are added to obtain the final solution.

$$V_O = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} + V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2}$$
(150)

The reader should analyze this circuit with loop or node equations to gain an appreciation for superposition. Again, the superposition results come out as a simple arrangement that is easy to understand. One looks at the final equation and it is obvious that if the sources are equal and opposite polarity, and $R_1 = R_3$, then the output voltage is zero. Conclusions such as this are hard to make after the results of a loop or node analysis unless considerable effort is made to manipulate the final equation into symmetrical form.

Calculation of a Saturated Transistor Circuit

The circuit specifications are: when $V_{IN} = 12$ V, $V_{OUT} < 0.4$ V at $I_{SINK} < 10$ mA, and $V_{IN} < 0.05$ V, $V_{OUT} > 10$ V at $I_{OUT} = 1$ mA. The circuit diagram is shown in Figure 14.
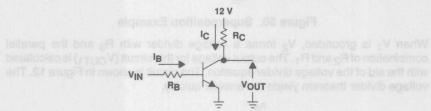
Figure 53. Saturated Transistor Circuit

The collector resistor must be sized when the transistor is off, because it has to be small enough to allow the output current to flow through it without dropping more than two volts.

$$R_C \le \frac{V_{+12} - V_{OUT}}{I_{OUT}} = \frac{12 - 10}{1} = 2 \text{ K} \tag{151}$$

When the transistor is off, 1 mA can be drawn out of the collector resistor without pulling the collector or output voltage to less than ten volts. When the transistor is on, the base resistor must be sized to enable the input signal to drive enough base current into the transistor to saturate it. The transistor beta is 50.

$$I_C = \beta I_B = \frac{V_{+12} - V_{CE}}{R_C} + I_L \approx \frac{V_{+12}}{R_C} + I_L \tag{152}$$

$$R_B \le \frac{V_{+12} - V_{BE}}{I_B} \tag{153}$$

Substituting equation 27 into equation 28 yields equation 29.

$$R_B \le \frac{(V_{+12} - V_{BE})\beta}{I_C} = \frac{(12 - 0.6)50}{\frac{12}{2} + (10)} = 35.6 \text{ K} \tag{154}$$

When the transistor goes on it sinks the load current, and it still goes into saturation. These calculations neglect some minor details, but they are in the 98% accuracy range.

Transistor Amplifier

The amplifier is an analog circuit, and the calculations, plus the points that must be considered during the design, are more complicated than for a saturated circuit. This extra complication leads people to say that analog design is harder than digital design (the saturated transistor is digital i.e.; on or off). Analog design is harder than digital design because the designer must account for all states in analog, whereas in digital only two states must be accounted for. The specifications for the amplifier are an ac gain of four and a peak-to-peak signal swing of 4 volts.
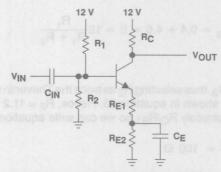
Figure 54. Transistor Amplifier

I_C is selected as 10 mA because the transistor has a current gain (β) of 100 at that point. The collector voltage is arbitrarily set at 8 V; when the collector voltage swings positive 2 V (from 8 V to 10 V) there is still enough voltage dropped across R_C to keep the transistor on. Set the collector-emitter voltage at 4 V; when the collector voltage swings negative 2 V (from 8 V to 6 V) the transistor still has 2 V across it, so it stays linear. This sets the emitter voltage (V_E) at 4 V.

$$R_C \leq \frac{V_{+12} - V_C}{I_C} = \frac{12 - 8}{10} = 400 \ \Omega \tag{155}$$

$$R_E = R_{E1} + R_{E2} = \frac{V_E}{I_E} = \frac{V_E}{I_B + I_C} \cong \frac{V_E}{I_C} = \frac{4}{10} = 400 \ \Omega \tag{156}$$

Use Thevenin's equivalent circuit to calculate R_1 and R_2 as shown in Figure 16.

Figure 55. Thevenin Equivalent of the Base Circuit

$$I_B = \frac{I_C}{\beta} = \frac{10 \ mA}{100} = 0.1 \ mA \tag{157}$$

$$V_{TH} = \frac{12R_2}{R_1 + R_2} \tag{158}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{159}$$

We want the base voltage to be 4.6 V because the emitter voltage is then 4 V. Assume a voltage drop of 0.4 V across R_{TH}, so equation 35 can be written. The drop across R_{TH} may not be exactly 0.4 V because of beta variations, but a few hundred mV does not matter is this design. Now, calculate the ratio of R_1 and R_2 using the voltage divider rule (the load current has been accounted for).

$$R_{TH} = \frac{0.4}{0.1} K = 4 \ K \tag{160}$$

$$V_{Th} - I_B R_{Th} + V_B = 0.4 + 4.6 = 5 = 12 \frac{R_1}{R_1 + R_2} \tag{161}$$

$$R_1 = \frac{7}{5} R_2 \tag{162}$$

R_1 is almost equal to R_2, thus selecting R_2 as twice the Thevenin resistance yields approximately 4 K as shown in equation 35. Hence, $R_2 = 11.2$ K and $R_1 = 8$ K. The ac gain is approximately R_C/R_{E1} so we can write equation 38.

$$R_{E1} = \frac{R_C}{G} = \frac{400}{4} = 100 \ \Omega \tag{163}$$

$$R_{E2} = R_E - R_{E1} = 400 - 100 = 300 \ \Omega \tag{164}$$

The capacitor selection depends on the frequency response required for the amplifier, but 10 μF for C_{IN} and 1000 μF for C_E suffice for a starting point.

Conclusions

The application note presents the minimum number of physics laws and equations required for beginning analog analysis. The laws and equations are simple, but when applied correctly, they are powerful. As you proceed further into the realm of analog analysis or into analog design, the physics laws and equations get more complicated, but they are understandable.

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Understanding Basic Analog – Active Devices

Application Report

Mixed Signal Products

SLOA026

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Understanding Basic Analog – Active Devices

By Ron Mancini

ABSTRACT

This application report describes active devices and their use as the basic building blocks of all electronic equipment. Active devices, coupled with passive devices, create the combination needed to fulfill all circuit requirements. A select few active devices are discussed in this report.

Introduction

Active devices have gain, thus they have transfer functions which are not available to passive devices. Active devices are considerably more complicated than passive devices; hence, their models and transfer equations are more complicated than those of passive devices. Active devices are the foundation on which all electronics equipment is built. Integrated circuits and higher forms of electronic components are built from the active devices discussed here.

Bipolar Junction Transistor

The bipolar junction transistor (BJT) was the first active semiconductor device manufactured; therefore, it became the workhorse of the semiconductor industry. When the field effect transistor (FET) manufacturing process was perfected, it began competing with the BJT. Since then, the FET has been taking sockets from the BJT, but there are many applications, such as high frequency amplifiers, where the BJT still excels. Also, the BJT manufacturing process can be simple and inexpensive, and this, coupled with the BJT's long list of captured sockets, insures that the BJT will be around for a long time.

BJT transistors are made from a silicon bar that has three areas that are doped differently to produce the transistor. Doping means that the base semiconductor material has charged atoms added to change its polarity. These three areas are called the base, emitter, and collector. The emitter and collector are doped to have the same polarity which can be positive or negative, and the base is doped to have the opposite polarity. The BJT, like most transistors, come in two types called NPN or PNP. P stands for positive, N stands for negative, and the positive or negative regions gain their name from the doping of the semiconductor material making up the base, collector, and emitter areas of the BJT. An NPN transistor has a positively doped base and a negatively doped collector and emitter.

An NPN transistor looks like two diodes with the anodes connected together (see Figure 1). The point where the anodes connect is called the base, one cathode is called the collector, and the other cathode is called the emitter. Although this illustration does not work with discrete diodes, it is fact in a BJT because when the width of the base junction is decreased enough, the back-to-back diodes function as a transistor. Using the back-to-back diode model, transistors are commonly checked for short circuits and open circuits with an ohmmeter. The base-emitter and base-collector junctions of a BJT act like forward biased diodes when the positive ohmmeter lead is connected to the base while the negative ohmmeter is connected to the emitter or collector. It looks like a reverse biased diode when the lead connections are reversed.

Figure 56. BJT Description

The model of a BJT is shown in Figure 2. The input circuit looks like a forward biased diode; the input impedance equation is $Z_{IN} = r_e = I_C/26$. The base-emitter junction must be forward biased, thus there is a forward voltage drop of V_{BE}. V_{BE} is approximately 0.6 volts in a silicon transistor, and 0.2 volts in a germanium transistor. The input current is called I_{base} or I_B.
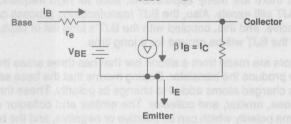
Figure 57. BJT Model

Since the collector-base junction is reverse biased, the collector current flows from the collector to the emitter. The collector current equation is $I_C = \beta(I_B)$ where β is the current gain of the transistor, and the emitter current equation is $I_E = I_C + I_B$. The impedance of the collector-emitter junction is called r_c, and r_c is very a high value (in the MΩ range). Current gain and the forward voltage drop are a function of the manufacturing process, temperature, and device physics, hence they are not stable parameters. Therefore, BJT circuits that depend on β and V_{BE} are not stable; thus, in well designed BJT circuits, the external components stabilize these parameters with feedback. This is not a drawback with just BJTs; this same condition exists for all transistors.

Junction Field Effect Transistor

The junction field effect transistor is called the JFET, and it comes in two flavors, p-channel and n-channel. It has high input impedance, so it is often used in the input circuit of amplifiers. The JFET has a high bandwidth, but circuit topologies and parasitic capacitors prevent it from achieving the same high bandwidth circuits where the BJT excels. Very often, the JFET is used as the input stage to achieve high input impedance. The JFET can achieve high bandwidth when its output is limited to small signal swings which are characteristic of input circuits. JFETs and BJTs can be made simultaneously on a semiconductor process called BIFET, thus they are often combined to make a high input impedance, high bandwidth amplifier. The JFET output impedance is high in the off state and low in the on state.

The JFET can be visualized as a bar of doped silicon that has a diode junction made in the middle of the bar. If the silicon bar is doped N, the JFET is called an N-channel device. Figure 3 shows the symbols for n-channel and p-channel JFETs. When the n-channel gate is negative with respect to the source the diode is biased off, the bar is depleted of carriers, and the source to drain resistance is quite high (several MΩ). When the n-channel gate is biased positive with respect to the source, the diode is biased on, and the bar is flooded with carriers thus causing a low source to drain resistance (as low as mΩ). The converse is true for a p-channel JFET.
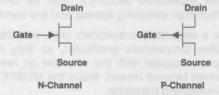

Figure 58. JFET Description

The linear JFET model is shown in Figure 4. When the JFET is biased in its linear region, the gate is represented as an open circuit because the input diode is reverse biased. The drain to source current is a voltage controlled current source, $g_m(e_g)$. The output resistance is modeled by R_O. As long as the signal swings stay in the linear region, the gate-source voltage signal swing induces a drain-source current flow. Again, as is the case with the BJT, the key parameters of the JFET such as gain are temperature and drift sensitive, so feedback is used to make JFET circuits dependent on stable passive components.
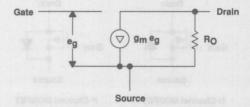

Figure 59. JFET Model

Metal Oxide Semiconductor Field Effect Transistors

The BJT and JFET have a diode in their input circuit which controls their mode of operation. The metal oxide semiconductor field effect transistor (MOSFET) works on a similar principle, but the diode is buried within the MOSFET. The MOSFET input diode is controlled by an electric field in the gate region, thus the input impedance is always extremely high because there is no forward biased diode to lower the input impedance. The input impedance of MOSFETs is so high that there is no mechanism that readily bleeds off the accumulated charge except for humidity, thus they are often packaged with lead shorting wires to drain the charge. The lead shorting devices protect the MOSFETs from charge buildup and the subsequent catastrophic discharge current. All semiconductor devices should be protected from static discharge, but MOSFETs are the most liable to build up a killing charge. Do not be lax with static protection because some sensitive BJTs are affected by only a few hundred volts static discharge.

The MOSFET is a majority carrier device, and because majority carriers have no recombination delays, the MOSFET achieves extremely high bandwidths and switching times. The gate is electrically isolated from the source, and while this provides the MOSFET with its high input impedance, it also forms a good capacitor. Driving the gate with a dc or a low frequency signal is a snap because Z_{IN} is so high, but driving the gate with a step signal is much harder because the gate capacitance must be charged at the signal rate. This situation leads to a paradox; the high input impedance MOSFET must be driven with a low impedance driver to obtain high switching speeds and low bandwidth.

MOSFETs do not have a secondary breakdown area, and their drain-source resistance has a positive temperature coefficient, so they tend to be self protective. These features, coupled with the very low on resistance and no junction voltage drop when forward biased, make the MOSFET an extremely attractive power supply-switching transistor.

The MOSFET (see Figure 5 for a description) can be visualized as a bar of doped silicon that contains a capacitively coupled diode junction in the middle of the bar. If the silicon bar is doped N, then the MOSFET is called an N-channel device. When the n-channel gate is charged negative with respect to the source the internal gate diode is biased off, the bar is depleted of carriers, and the source to drain resistance is quite high (several hundred MΩ). When the n-channel gate is charged positive with respect to the source, the internal gate diode is biased on, and the bar is flooded with carriers thus causing a low source to drain resistance (in the low mΩ range). The converse is true for a P-channel MOSFET.
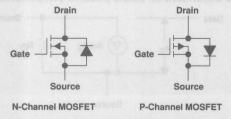

N-Channel MOSFET   **P-Channel MOSFET**

Figure 60. MOSFET Description

The linear MOSFET model is shown in Figure 6. When the MOSFET is biased in its linear region, the gate appears as an open circuit to dc. The drain to source current is derived from a voltage controlled current source, $g_m(e_g)$. The output resistance is modeled by R_O. As long as the signal swings stay in the linear region, gate-source voltage signals induce a drain-source current.
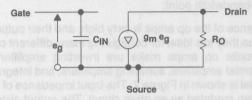

Figure 61. MOSFET Model

The MOSFET contains a diode connected across from the drain (cathode) to the source (anode). This diode is not forward biased during normal operation, consequently it does not conduct current during normal operation. When the MOSFET is connected to an inductive load, the inductive kick causes the diode to turn on and conduct current. In some modes of operation, this is a desired effect because it limits the inductive voltage rise. The diode is not a fast turn-off diode, so it consumes quite a bit of power during turn-off. The turn-off power consumption is detrimental in some circuits, thus those circuits must put a diode with a smaller forward voltage drop (Schottky diode) in parallel with the body diode.

C_{IN} can be as large as several hundred pF, and it must be charged by the gate signal. When the MOSFET is used in a power switching application, the gate is normally driven by a low impedance driver so that C_{IN} can be charged quickly. If C_{IN} is charged slowly, the switching time of the MOSFET is long causing the MOSFET to stay in the linear region for a long time. When the MOSFET operates in the linear region, its voltage drop and current flow are high, resulting in high power dissipation.

Again, as is the case with the BJT, the key parameters of the MOSFET such as gain are temperature and drift sensitive, so feedback is used to make MOSFET circuits dependent on stable passive components.

Voltage Feedback Operational Amplifier

The voltage feedback operational amplifier (VF op amp), or op amp as it is affectionately known, is a versatile amplifier which requires feedback to function. The op amp gain is so high that the output saturates on any differential input signal, so feedback is employed to lower the closed loop gain. The feedback makes the op amp circuit a precision circuit because the closed loop gain is dependent on the passive components which can be very accurate. Some op amp parameters, such as input offset voltage can still degrade precision, but there are specially designed precision op amps that have very low input offset voltages (micro volts), and selected salient parameters chosen to yield a precision circuit. The differential input structure of op amp enhances precision because the transistors in both inputs can be matched.

Op amp bandwidth depends on the process used to make the op amp, and BJT op amps have the highest bandwidth and current drain, with JFET op amps are next highest, and MOSFET op amps have the lowest bandwidth and current drain. Voltage feedback op amps are discussed in this section, and their bandwidth starts rolling off at low frequencies (about five decades before the advertised gain–bandwidth point.

The input impedance of the op amps is very high, and their output impedance is relatively low, thus they are ideal for configuring many different circuits. Some of the possible circuits op amps make are inverting amplifiers, noninverting amplifiers, differential amplifiers, summing amplifiers, and integrating amplifiers. The op amp model is shown in Figure 7. The input impedance of op amps is very high, and it is often modeled as an open circuit. The output circuit consists of a voltage controlled voltage source, and the control voltage is the differential voltage applied across the inputs.
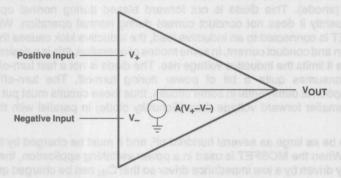

Positive Input —— V_+

V_{OUT}

$A(V_+–V_–)$

Negative Input —— $V_–$

Figure 62. Voltage Feedback Op Amp Model

Op amps are always surrounded with passive components, which are required to program the gain and add stability.

Current Feedback Operational Amplifiers

Current feedback op amps, called CFA for current feedback amplifier, are also called op amps, hence there can be confusion about which type of op amp (voltage or current feedback) is under discussion. It is assumed that voltage feedback op amps are being discussed unless a reference is made to the current feedback op amp (CFA).

The CFA configuration makes it hard to achieve precision because there is a buffer tied across the inputs. The input structure of a CFA is not matched, hence it is hard to obtain dc precision, which requires a matched input structure (usually a differential amplifier is used when matching is required). The applications for CFAs generally do not require high precision because CFAs are used in high frequency circuits. In many high frequency circuits, the dc portion of the signal contains little or no information, thus precision is not paramount in these applications.

CFAs are usually made with BJTs because they yield very high bandwidths. The high bandwidth of a CFA does not start rolling off till much higher frequencies (several decades higher) than a VFA does, but it rolls off at a much faster rate. CFA have bandwidths in the GHz range while VFA bandwidths are down in the several hundred MHz range. The input impedance of CFAs is high for the positive input and low for the negative input because of the input voltage buffer.

The CFA model is shown in Figure 8. The positive input is a voltage buffer input, so the positive input has very high input impedance. The negative input is connected to the output of the same voltage buffer, hence the negative input impedance is close to zero. It is very hard to match parameters between the inputs because they are connected to different ends of a buffer, and this situation makes it hard to build precision CFAs.
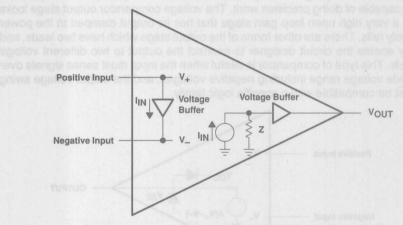
Figure 63. Current Feedback Op Amp Model

The output circuit contains a transimpedance stage, Z, so the error current which flows through the input stage I_{IN} is multiplied by Z to form a voltage. This voltage is buffered before it becomes the output voltage, thus the CFA has very low output impedance.

Voltage Comparators

The voltage comparator is used to convert an analog signal to a digital signal. This is usually accomplished by connecting a reference to the negative comparator input and a signal to the positive comparator input. When the signal exceeds the reference the output goes from a low voltage (a logic zero) to a high voltage (a logic one). Inverted operation can be obtained with a comparator by reversing the inputs.

The input stage of a comparator is similar to an op amp input stage. The differential input voltage is multiplied by the gain to obtain an output signal. The comparator gain is very large, and it is not limited by feedback, so the output would saturate if it was an op amp. The difference is that the comparator has an output stage that reaches a limit but does not saturate. The comparator's ability to run open loop without saturating separates it from the op amp which always saturates when it runs open loop. Never use op amps for a comparator function when propagation delay is important, because when an op amp saturates, the time needed for it to come out of saturation is unpredictable.

The voltage comparator is shown in Figure 9. The voltage comparator input stage is identical to a VF op amp input stage, consequently the comparator input impedance is very high. The inputs can be matched very well, thus comparators are capable of doing precision work. The voltage comparator output stage looks like a very high open loop gain stage that has its output clamped to the power supply rails. There are other forms of the output stage which have two leads, and they enable the circuit designer to connect the output to two different voltage levels. This type of comparator is useful when the input must sense signals over a wide voltage range including negative voltages, and the output voltage swing must be compatible with a specific logic family.
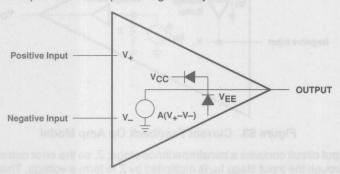
Figure 64. Voltage Comparator Model

Other Active Devices

There are many more active devices than are covered in this application report. The exposure here is limited to the most popular devices, and these devices are adequate to cover the large majority of electronic equipment applications.

Specialty fields like power supplies, motor controls, data transmission, etc. have active devices not shown here. Rather than turn this application report into a two hundred-page collection of active devices, 99 percent of which are of little or no interest to the average reader, the author chose to ignore 99 percent. If you have a need for further information on an active device, mentioned or not mentioned here, contact the manufacturer. For example, if you contact the local TI sales office or the factory in Dallas, and ask for information on current feedback op amps, TI will send you information gratis. If you contact the local analog field specialist, they will see that you are sent data sheets and applications literature.

This application note is purposely kept brief, but the manufacturer's support system is more than happy to flood you with information. If you can't get information from a manufacturer, maybe you are talking to the wrong manufacturer.

Summary

Active devices have gain, so they perform functions that passive devices can't fill. Active devices have voltage, current, and power gain; hence, when active devices are coupled with passive devices the combination fulfills all circuit requirements.

Active devices employ feedback to control the gain, and the feedback makes active devices dependent on passive device parameters. Accept this for now, because later applications will illustrate the concept. Feedback brings its own problems as well as its advantages. Oscillation resulting from misapplied feedback is the major disadvantage of active circuits.

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Contents

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Mechanical Data

Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as shown in the following example.

Example: **TLE** **2022** **PW** **LE**

Prefix

MUST CONTAIN TWO OR THREE LETTERS

TL, TLE .... TI Linear Products
TLC .... TI Linear Silicon-Gate CMOS Products
TLV .... TI Low-Voltage CMOS Products

STANDARD SECOND-SOURCE PREFIXES

AD .... Analog Devices
LF, LM, or LP .... National
LT .... Linear Technology
MC .... Motorola
NE, SA, or SE .... Signetics
OP .... PMI
RC, RM, or RV .... Raytheon
uA .... Fairchild/National

Unique Part Number

MUST CONTAIN TWO OR MORE CHARACTERS
(from individual data sheets)

Examples: 10   34070
            592   1451AC
            7757   2217-285

Package

MUST CONTAIN ONE, TWO, OR THREE LETTERS

D, DB, DBV, DGK, DGN, DGQ, DGS, DW, DWP, FK, J, JG, N, NE, P, PW, PWP, U, W
(from pin-connection diagrams on individual data sheet)

Available Taped and Reeled or Left-Ended Taped and Reeled

R – Available Taped and Reeled
LE – Available Only Left-Ended Taped and Reeled

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ORDERING INSTRUCTIONS

Circuits are shipped in one of the carriers below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped via the most practical carrier.

Dual-In-Line (J, JG, N, NE, P)
 – A-Channel Antistatic or
   Conductive Plastic Tubing

Small Outline (D, DW, DWP)
 – Tape and Reel
 – Antistatic or Conductive
   Plastic Tubing

Shrink Small Outline (DB, DBV)
 – Tape and Reel
Thin Shrink Small Outline (PW)
 – Tape and Reel

Chip Carriers (FK)
 – Antistatic or Conductive
   Plastic Tubing

Flat (U, W)
 – Milton Ross Carriers
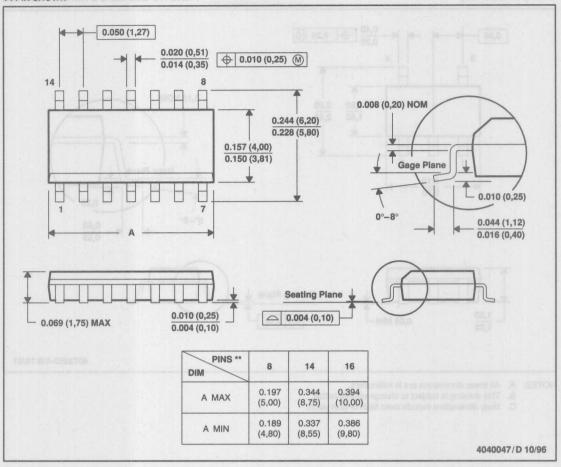
PACKAGE GUIDE

INDUSTRY STANDARD PACKAGE	TI PACKAGE SUFFIX	NUMBER OF PINS
SOT-23	DBV	5, 6 (Shutdown)
MSOP	DGK	8
	DGN	8 (PowerPAD™)
	DGS	10
	DGQ	10
TSSOP	PW	8, 14, 16, 20, 24, 28
	PWP	20 (PowerPAD™)
SOIC	D	8, 14, 16
	DW	16, 20, 24, 28
	DWP	16, 20, 24, 28 (PowerPAD™)
PDIP	P	8
	N	14, 16, 18, 20
	NE	16, 20
SSOP	PS	8

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D (R-PDSO-G**)
14 PIN SHOWN

PLASTIC SMALL-OUTLINE PACKAGE

PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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MECHANICAL DATA

MECHANICAL INFORMATION

DBV (R-PDSO-G5)   PLASTIC SMALL-OUTLINE PACKAGE

4073253-4/B 10/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

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MECHANICAL INFORMATION

DBV (R-PDSO-G6)   PLASTIC SMALL-OUTLINE PACKAGE

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions include mold flash or protrusion.

4073253-5/B 10/97

MECHANICAL DATA
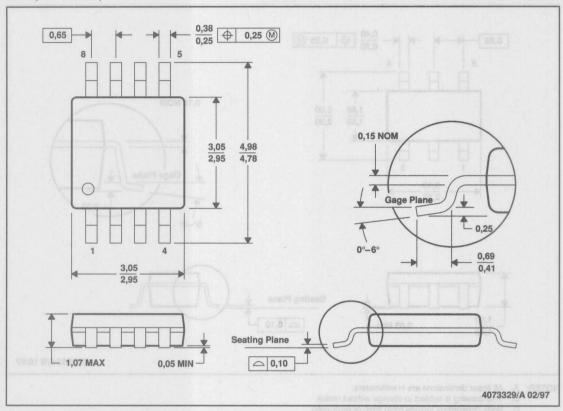
DGK (R-PDSO-G8)   PLASTIC SMALL-OUTLINE PACKAGE
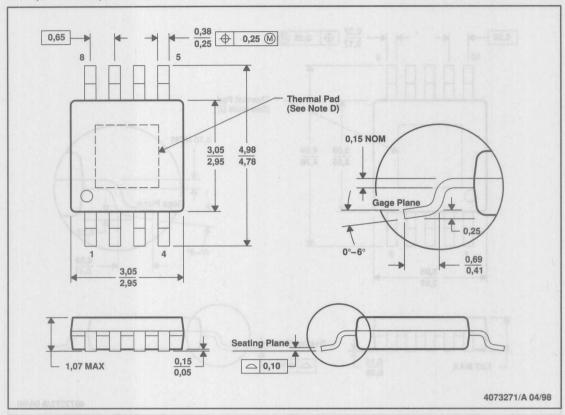
4073329/A 02/97

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

DGN (S-PDSO-G8)   PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE

4073271/A 04/98

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions include mold flash or protrusions.
        D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad.
            This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimension of the thermal pad is 68 mils (height as illustrated) × 70 mils (width as illustrated) (maximum). The pad is centered on the bottom of the package.
        E. Falls within JEDEC MO-187
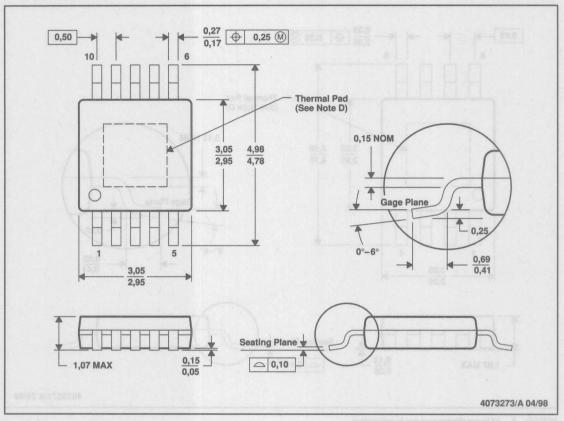
PowerPAD is a trademark of Texas Instruments Incorporated.

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MECHANICAL DATA

MECHANICAL INFORMATION

DGQ (S-PDSO-G10)   PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE
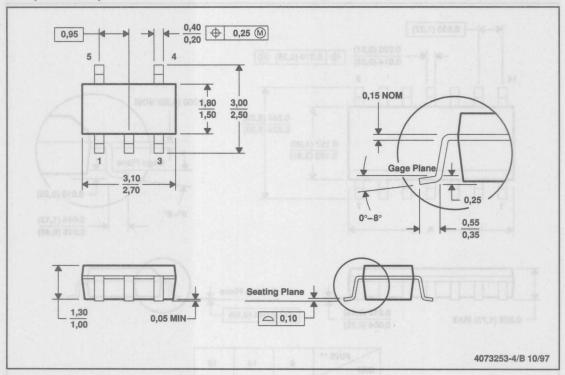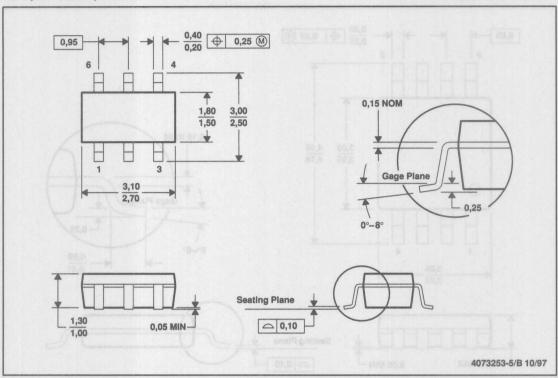

NOTES: A. All linear dimensions are in millimeters.
       B. This drawing is subject to change without notice.
       C. Body dimensions do not include mold flash or protrusion.
       D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
          This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimension of the thermal pad is 68 mils (height as illustrated) × 70 mils (width as illustrated) (maximum). The pad is centered on the bottom of the package.
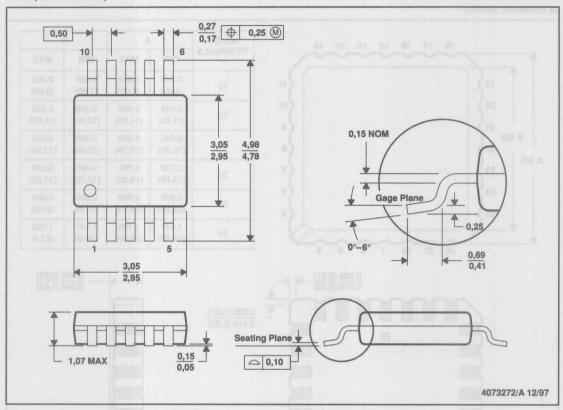
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MECHANICAL INFORMATION

DGS (S-PDSO-G10)   PLASTIC SMALL-OUTLINE PACKAGE
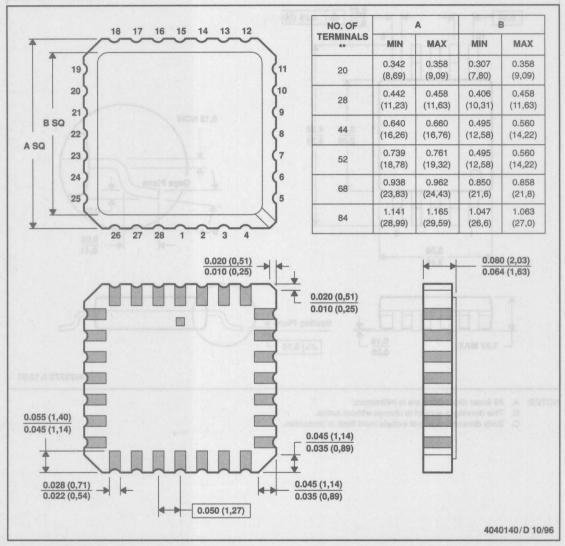

4073272/A 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

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MECHANICAL DATA

MECHANICAL INFORMATION

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	**MAX**	**MIN**	**MAX**
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS

MECHANICAL INFORMATION

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

14 LEADS SHOWN

DIM \ PINS **	14	16	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)

0.065 (1,65) / 0.045 (1,14)

0.100 (2,54) / 0.070 (1,78)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.023 (0,58) / 0.015 (0,38)

0.100 (2,54)

A

0°–15°

0.014 (0,36) / 0.008 (0,20)

4040083/E 03/99

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, and GDIP1-T20

TEXAS INSTRUMENTS

MECHANICAL DATA

MECHANICAL INFORMATION

JG (R-GDIP-T8)   CERAMIC DUAL-IN-LINE PACKAGE

0.400 (10,20)
0.355 (9,00)

8   5

0.280 (7,11)
0.245 (6,22)

1   4

0.065 (1,65)
0.045 (1,14)

0.310 (7,87)
0.290 (7,37)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.063 (1,60)
0.015 (0,38)

0.023 (0,58)
0.015 (0,38)

0.100 (2,54)

0°–15°

0.014 (0,36)
0.008 (0,20)

4040107/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
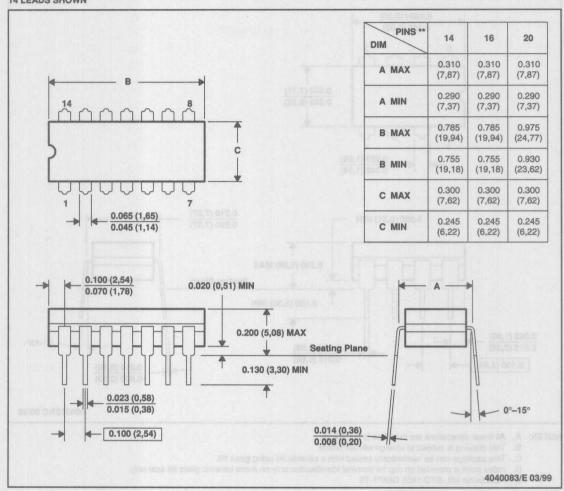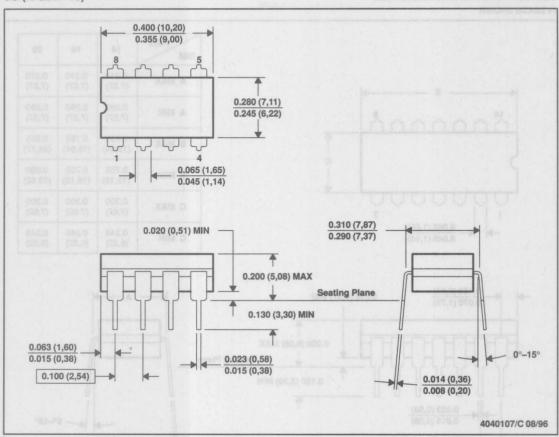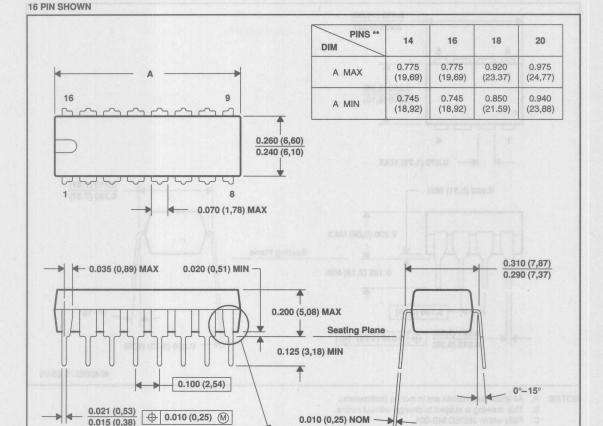   C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E. Falls within MIL-STD-1835 GDIP1-T8

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MECHANICAL INFORMATION

N (R-PDIP-T**)   PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78) MAX

0.035 (0,89) MAX   0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)   ⊕ 0.010 (0,25) Ⓜ

0.310 (7,87)
0.290 (7,37)

0°–15°

0.010 (0,25) NOM

14/18 PIN ONLY

4040049/C 08/95

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

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MECHANICAL DATA

MECHANICAL INFORMATION

P (R-PDIP-T8)   **PLASTIC DUAL-IN-LINE PACKAGE**

0.400 (10,60)
0.355 (9,02)

0.260 (6,60)
0.240 (6,10)

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)   ⊕ 0.010 (0,25) Ⓜ

0.310 (7,87)
0.290 (7,37)

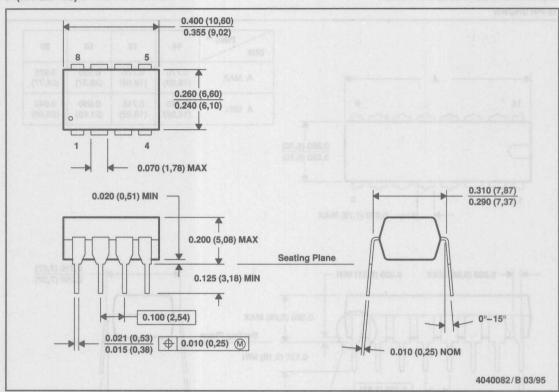0°–15°

0.010 (0,25) NOM

4040082 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MS-001

TEXAS INSTRUMENTS

MECHANICAL INFORMATION
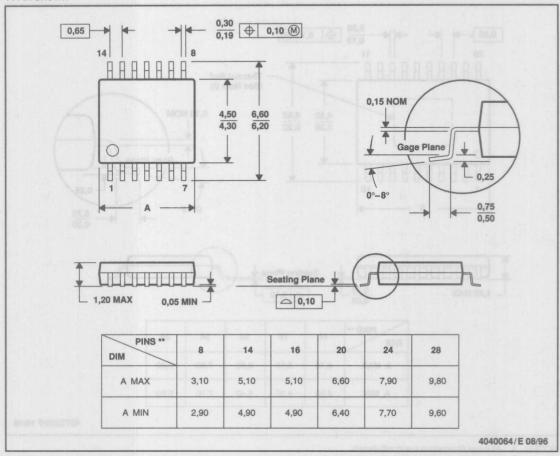
PW (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

DIM / PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064 / E 08/96

NOTES: A. All linear dimensions are in millimeters.
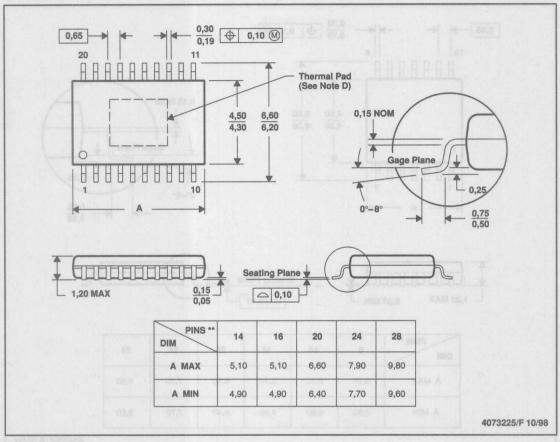　　　　B. This drawing is subject to change without notice.
　　　　C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
　　　　D. Falls within JEDEC MO-153

MECHANICAL DATA

MECHANICAL INFORMATION

PWP (R-PDSO-G**)   **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN

PINS ** DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusions.
        D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane.
            This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
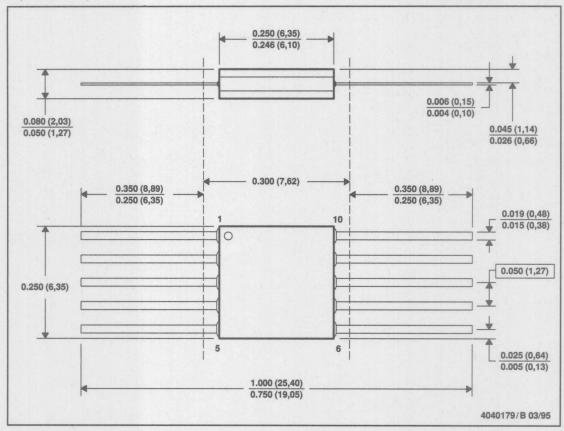   E. Falls within JEDEC MO-153

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MECHANICAL INFORMATION

U (S-GDFP-F10)   CERAMIC DUAL FLATPACK

0.250 (6,35)
0.246 (6,10)

0.080 (2,03)
0.050 (1,27)

0.006 (0,15)
0.004 (0,10)

0.045 (1,14)
0.026 (0,66)

0.350 (8,89)
0.250 (6,35)

0.300 (7,62)

0.350 (8,89)
0.250 (6,35)

0.019 (0,48)
0.015 (0,38)

1   10

0.050 (1,27)

0.250 (6,35)

5   6

0.025 (0,64)
0.005 (0,13)

1.000 (25,40)
0.750 (19,05)

4040179 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
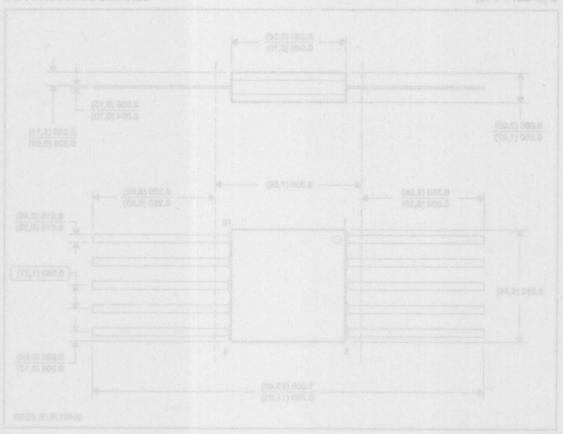   D. Index point is provided on cap for terminal identification only.
        E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

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MHT000101D – JANUARY 1986 – REVISED MAY 1996

MECHANICAL INFORMATION

U (S-GDFP-F10)   CERAMIC DUAL FLATPACK

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only.
        E. Falls within MIL-STD-1835 GDFP1-F10 and JEDEC MO-092AA.